AEC - Q002 Rev B
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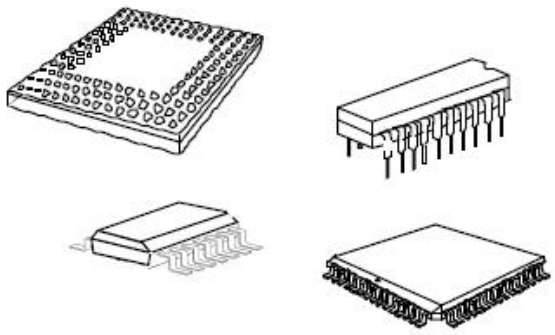
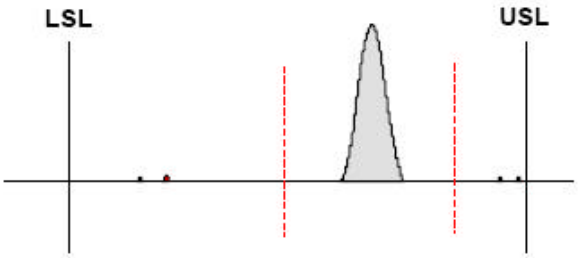
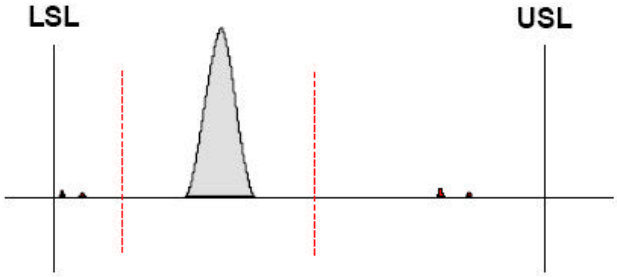
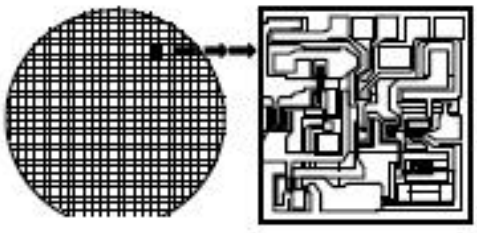
Automotive Electronics Council
Component Technical Committee





GUIDELINES FOR STATISTICAL YIELD ANALYSIS





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Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development and release of this document:

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GUIDELINES FOR STATISTICAL YIELD ANALYSIS

Text enhancements and differences made since the last revision of this document are shown as underlined text.

1. SCOPE

This guideline is intended for use as a method for detecting and removing abnormal lots of material and thus ensuring the quality and reliability of the ICs supplied as meeting AEC-Q100 or AEC-Q101. The principles described in this guideline are applicable to packaged or unpackaged die.

1.1 Purpose

This guideline describes a method, utilizing statistical techniques based on statistical yield limits (SYL) and statistical bin limits (SBL) statistical computations, of identifying a wafer, wafer lot, or assembly lot that exhibits an unusually low yield or an unusually high bin failure rate. Experience has shown that wafer and assembly lots exhibiting these abnormal characteristics tend to have generally poor quality and can result in significant system reliability and quality problems.

The exact methods applied may vary from what is described in this guideline, specifically if distributions are non-normal. Such derived methods may be employed with good statistical justification. The supplier shall be prepared to justify the statistical approach used.

Note: For best SYL and SBL results, use test limits based on Part Average Testing Limits (PAT) as described in AEC Q001.

1.2 References

AEC-Q001 Guidelines for Part Average Testing
AEC-Q100 Stress Test Qualification for Integrated Circuits
AEC-Q101 Stress Test Qualification for Discrete Semiconductors

2. METHOD FOR ESTABLISHING STATISTICAL YIELD LIMITS (SYL) AND STATISTICAL BIN LIMITS (SBL)

2.1 Detailed Description for Basic Wafer / Wafer Lot / Assembly Lot Level Yield Limits

Collect data from at least six lots and characterize the nature of the statistical distribution for yield (good die per wafer) and for all critical fail bins, as determined between the supplier and user/customer (number of die failing for each fail bin cause). If the yield and fail bin distributions show a reasonable fit to a normal distribution (normal distribution is applicable), determine the mean and sigma value for the percentage of devices passing per lot and the percentage of devices failing each bin-out per lot (lot as used here could mean each wafer, a wafer lot or an assembly lot).

Early in production of a part, when data from six lots is not available, data from characterization/matrix lots, similar to existing products and design simulation, may be used to set preliminary limits. The preliminary limits shall be updated as soon as current production data becomes available. The review and update should be performed periodically using current production data during the first 6 months of production. This initial update exercise should be done with a frequency based on product ramp rate as is practical, such as after every 2 diffusion lots or every 30 days.

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The current data used shall include the data available since the last update or at least the last 8 lots. Older data shall not be used. After the first 6 months of production the limits shall be updated at least twice per year or as agreed between supplier and user/customer. With this data determine the SYL and SBL (both on a wafer, wafer lot and assembly lot basis) as follows:

SYL_1 = Mean - 3 Sigma
SBL_1 = Mean + 3 Sigma

SYL_2 = Mean - 4 Sigma
SBL_2 = Mean + 4 Sigma

If the statistical distribution of good die per wafer or fail bin die/wafer does not fit a normal distribution, the supplier may use alternative methods. This may include transforming the data through mathematical manipulation so the normal distribution is applicable or fitting the data to another suitable distribution (Weibull, Gamma, Poisson, etc.) and establish SYL/SBL limits to achieve the same risk probabilities as one would achieve at 3s or 4s for a normal distribution. Any other method may be employed with good statistical justification. The supplier shall be prepared to justify the statistical approach used.

Any wafer or lots that fall below SYL_1 or exceed SBL_1 shall be flagged for engineering review. In addition, lots that fall below SYL_2 or exceed SBL_2 may be quarantined. Supplier shall perform a risk assessment for disposition of quarantined material. Containment actions shall be taken to reduce risk to user/customer. Material below minimum yield threshold or with high reliability risk shall be scrapped. For major excursions, supplier shall determine the root cause, corrective action, and future prevention. For any lots outside of the limits that will be shipped, notification per established agreement between supplier and user/customer shall be given.

2.2 Records

The supplier shall maintain records on all wafers, wafer lots and assembly lots that fall below SYL_2 or exceed SBL_2. This data shall include the root cause for the yield problem and corrective action taken to prevent reoccurrence of the problem. It should also include any special testing or screens that were performed on the wafer, wafer lot, or assembly lot and the customer that approved the shipment of the parts in question. The supplier shall apply their policy for records retention to these results.

3. CUSTOMER NOTIFICATION

3.1 Procedure for Customer Notification

Before the user/customer is notified, the supplier shall have determined the failure mechanism(s) and, based on his experience, determine the corrective action required to prevent a reoccurrence of the condition in future product. The supplier shall also present data on a reasonable expectation of the seriousness of the failure mechanism(s) and its impact on quality and reliability. Included in this data should be a plan for additional tests and screens which could provide the user/customer with reasonable certainty that the product he receives will be at least equal to normal product.

3.2 Procedure for Customer Notification Through Distribution Network

If the supplier is unaware of the user/customer, in the case of the user/customer purchasing parts through distribution, then the supplier must maintain records of disposition for the lots falling below SYL_2 or exceeding SBL_2 that have been shipped to distributors. Any user/customer, purchasing through a distribution network, must understand that parts purchased from distribution may not meet AEC-Q002, unless prior agreement has been reached between supplier and user/customer.

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	July 31, 1997	Initial Release.
A	Aug. 25, 2000	Added Paragraph 1.2. Revised Paragraphs 1, 2.1, and 4.3.
B	Jan. 12, 2012	Complete Revision. Added Notice Statement. Revised (and renumbered where appropriate) Acknowledgement and Sections 1.1, 1.2, 3, 3.1, 3.2, 4, 4.1, and 4.3. Deleted signature block and Sections 2, 2.1, and 4.2.

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