Automotive Electronics Council
Component Technical Committee

ATTACHMENT 5

AEC - Q100-005 - REV-D1

NON-VOLATILE MEMORY PROGRAM/ERASE ENDURANCE, DATA RETENTION, AND OPERATING LIFE TEST

Automotive Electronics Council

Component Technical Committee

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document:

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Change Notification

The following summary details the changes incorporated into AEC-Q100-005 Rev-D1:

- Section 1, Purpose: Added note addressing One-Time Program (OTP) Non-volatile memories.
- Section 3.1.c, Program/Erase Endurance Cycling Procedure: Added rules for Checkerboard/Inverse-Checkerboard cycling.
- Section 3.3, Post-Cycled Low Temperature Data Retention (LTDR) Procedure: Added new subsection (c).
- Appendix B: Added new captions for Tables B1 and B2. Corrected Table values.

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METHOD - 005

NON-VOLATILE MEMORY PROGRAM/ERASE ENDURANCE, DATA RETENTION, AND OPERATING LIFE TEST

Text enhancements and differences made since the last revision of this document are shown as underlined text.

1. PURPOSE

This test is intended to evaluate the ability of the memory array of a standalone Non-volatile Memory (NVM) integrated circuit or an integrated circuit with a Non-volatile Memory module (such as a microprocessor Flash Memory) to: sustain repeated data changes without failure (Program/Erase Endurance), retain data for the expected life of the Non-volatile Memory (Data Retention), and withstand constant temperature with an electrical bias applied (Operating Life).

Alternative procedures requested by the NVM supplier, including but not limited to program/erase cycle sequencing, data retention duration and temperature, and checksum testing on stand-alone NVM devices, must be approved by the user.

For Program/Erase Endurance Cycling, a data change occurs when a stored "1" is changed to a "0", or when a stored "0" is changed to a "1". Failure occurs when a write or erase event is not completed in less than the maximum specified time, or when the event completes but the data pattern within the memory array does not correspond to the intended data pattern.

Data Retention is a measure of the ability of a memory cell in an NVM array to retain its charge state in the absence of applied external bias. Data retention failure occurs when a memory cell loses or gains charge to the extent that it is no longer detected to be in its intended data state.

A bit flip is defined as the failure of a bit to retain its data state after a program or erase operation.

Three categories of failure can occur due to Operating Life stress. The Non-volatile Memory may exceed its parametric limits, it may no longer meet the device specification requirements, or it may fail to retain its intended data state.

Note that OTP (One-Time Program) Non-volatile Memories are a special case and certain sections of this test method may not be applicable. The same may apply for memories serving as an integral part of a device's operation. The supplier and user should mutually agree on testing to be performed for these special cases.

2. APPARATUS

The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the temperature conditions at or above the specified temperatures (e.g., 125°C -0/+5°C chamber tolerance). Sockets or other mounting means shall be provided within the chamber so that reliable electrical contact can be made to the device terminals in the specified circuit configuration. Power supplies and biasing networks shall be capable of maintaining the specified operating conditions throughout the test. Also, the test circuitry shall be designed so that the existence of abnormal or failed devices will not alter the specified conditions for other units on test. Care shall be taken to avoid possible damage from transient voltage spikes or other conditions which might result in electrical, thermal or mechanical overstress.

3. PROCEDURE

Devices containing NVM shall first be preconditioned (exercised) through the Program/Erase Endurance test before performing High Temperature Data Retention (HTDR), High Temperature Operating Life (HTOL) and Low Temperature Data Retention (LTDR) testing (see Figures 1 and 2):

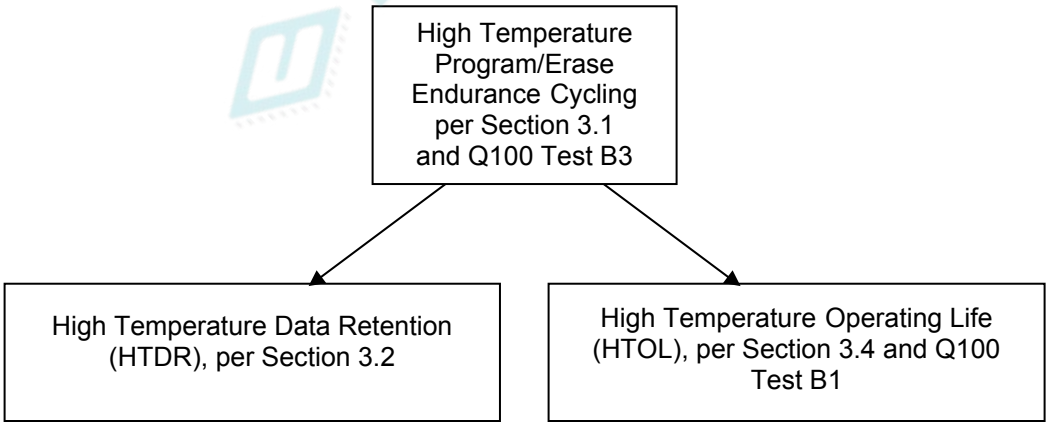

Figure 1: High Temperature Test Sequence for Devices Containing NVM

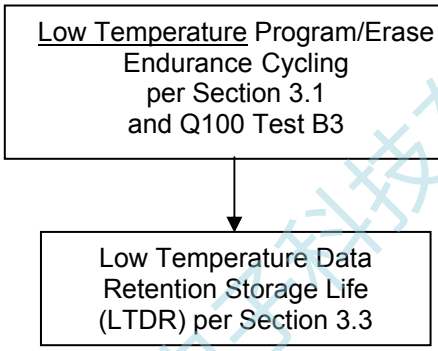

Figure 2: Low Temperature Test Sequence for Devices Containing NVM

Separate testing for high temperature and low temperature degradation processes is required since, while some degradation processes are accelerated by temperature, other degradation processes (e.g., Stress Induced Leakage Current (Flash-SILC)) heal with temperature and may not show up in the high temperature flow.

With user approval, the supplier is allowed to reduce the size of the NVM array being preconditioned or endurance tested to reduce qualification time to a reasonable length. In such instances the program/erase cycles applied to the reduced memory must be no less than the maximum specification. The size of the reduced memory array shall represent the amount typically used in high endurance applications. The remaining array segments shall be preconditioned or endurance tested to the maximum number of program/erase cycles possible without adding unreasonable qualification time. Program/erase cycling shall follow the requirements of this document outlined in Section 3.1.

3.1 Program/Erase Endurance Cycling Procedure

a. Devices shall be placed in the chamber so there is no substantial obstruction to the flow of air across and around each unit. The power shall be applied and suitable checks made to ensure that all devices are properly energized. When special mounting or heat sinking is required the details shall be specified in the applicable device specification.

b. Devices shall be tested for Program/Erase Endurance Cycling using the minimum number of cycles stated in the applicable device specification. Endurance testing shall be performed using the following conditions with respect to temperature and cycling frequency:

1. *High Temperature Cycling*: Cycling shall be performed at temperature T ≥ 85°C, with total cycling time not exceeding 15% of the accelerated product life. See Appendix A for an example of calculating maximum cycling time at selected cycling stress temperature.

   Delays in between cycles or between groups of cycles are allowed as long as the delays are spread evenly over the cycling period and the total cycling duration, including delays, does not exceed above rule.

2. *Low Temperature Cycling:* Cycling shall be performed at temperature of T≤ 55°C

   Delays in between cycles or between groups of cycles are allowed as long as the delays are spread evenly over the cycling period, and the total cycling duration, including delays, does not exceed 15% of product life.

c. Cycling is performed continuously, with one cycle being defined as a transition from one state to another and back to the original state (i.e., from “1” to “0” and back to “1”; or from “0” to “1” and back to “0”) on all bit cells in the memory array. During the endurance test, each program and erase operation must be verified to have successfully completed and the intended data state is to be validated through a read operation. Endurance test cycling is described below.

Possible cycling patterns may include the following sequences:

1. **Checkerboard cycling:**
   - Program array checkerboard
   - Normal read array checkerboard
   - Erase array
   - Normal read array all “1”

2. **All “0”/All “1” cycling:**
   - Program array all “0”
   - Normal read array all “0”
   - Erase array
   - Normal read array all “1”

3. **Checkerboard/Inverse-Checkerboard cycling:**
   - Odd cycles: Program array checkerboard
   - Normal read array checkerboard
   - Erase array
   - Normal read array all "1"
   - Even cycles: Program array inverse-checkerboard
   - Normal read array inverse-checkerboard
   - Erase array
   - Normal read array all "1"

   Note; Flow #3 should be applied when over-program or over-erase is not a concern, but when interaction between bits may occur.

Alternate program/erase algorithms or patterns could be used upon agreement between the supplier and user.

For large array sizes at least one-third of the total cycling time should be spent on blocks cycled to full-array endurance specification, one-third of the total cycling time should be spent on blocks cycled to 10% of the full-array endurance specification, and the rest of the cycling time should be spent on cycling the rest of the array. For memory devices employing on-the-chip Wear Leveling (WL) algorithm, which force all blocks to cycle evenly, the WL algorithm must be disabled such that cells in the array can be stressed to the array specification. If this is not possible, supplier and user must agree on an alternative stressing procedure.

For devices containing memory that uses error correction code (ECC) for fault tolerance, this coding algorithm must be disabled such that all cells in the array can be stressed and tested without the effect of error correction techniques.

However, for memories with very large array size, devices with deeply scaled technology or devices designed with built-in ECC, supplier can request user approval to perform cycling in user mode (ECC active). In the later case, upon user request, supplier shall provide test data that deactivates/bypasses the ECC operation, to allow extrapolation of bit error rates to extreme conditions".

d. Following completion of the specified number of Program/Erase cycles, verification of functionality to the device specification shall be performed per Section 3.6.

3.2 Post-Cycled High Temperature Data Retention (HTDR) Procedure

a. After completing Program/Erase Endurance Cycling testing as described in Section 3.1, the devices shall be programmed with a worst-case pattern for the specific technology, such as topological checkerboard (i.e., where each bit is surrounded by its complement) or all bit cells programmed. Alternative patterns are acceptable when agreed to by the user and supplier. With user acceptance, data may also be written using a mode of programming that is different from that specified in the datasheet, to modify the margins of the cells and obtain additional acceleration. For multi-level-cell (MLC) memories, the pattern must include all possible combinations of cell + cell nearest neighbor combinations.

b. The units cycled at high temperature per Section 3.1.b.1 are subjected to High Temperature Data Retention test (HTDR) according to their specified grade and according to their intended user-specified mission profile. Data retention bake duration and temperature are determined from the user-specified mission profile and the technology's activation energy for data retention as described in Appendix B.

c. To preserve the intent of the Data Retention stress, only data pattern verification and non-array altering functional testing is performed at interim read points. This purposely excludes any program or erase testing of the NVM array.

d. At the qualification time-point, devices are first tested to verify that the data pattern has been retained at temperature(s) justified by the supplier. This is to be followed by full functional testing to the device specification, per AEC-Q100 test B3. At this point, full functional testing consists of array altering program and erase events.

e. If High Temperature Storage Life (HTSL) stress test per Table 2 of AEC-Q100 is performed on devices cycled according to Section 3.1.b.1, the HTSL test qualifies the product also for HTDR, and there is no need for a separate HTDR test. This applies only if the HTSL bake period required to qualify the product for the specified grade and user mission profile is no less than the bake period required to qualify HTDR, as demonstrated in Appendix B below. The user shall specify the requested time/temperature mission profile that both HTDR and HTSL must meet.

3.3 Post-Cycled Low Temperature Data Retention (LTDR) Procedure:

a. After completing Program/Erase Endurance Cycling testing as described in Section 3.1, the devices shall be programmed with a worst-case pattern for the specific technology, such as topological checkerboard (i.e., where each bit is surrounded by its complement) or all bit cells programmed. Alternative patterns are acceptable when agreed to by the user and supplier. With user acceptance, data may also be written using a mode of programming that is different from that specified in the datasheet, to modify the margins of the cells and obtain additional acceleration. For multi-level-cell (MLC) memories, the pattern must include all possible combinations of cell + cell nearest neighbor combinations.

b. The units cycled at low temperature per Section 3.1.b.2 are subjected to maximum 55°C Storage for minimum of 1000 hours. Per user request, supplier shall provide extrapolated results based on parametric data traced at logarithmic time intervals (e.g. 10hr, 100hr, 1000hr etc.). Preferably, bit-threshold-voltage or read current degradation rate shall be traced, and worst bit per unit per sample should be demonstrated to pass at specified product life. For large devices, on which it is not practical to collect parametric degradation data of all bits, a statistically viable bit ensemble should be selected, and supplier should justify the selection of the bit ensemble.

c. See Sections 3.2.c and 3.2.d for additional steps.

3.4 High Temperature Operating Life (HTOL) Procedure

a. After performing Program/Erase Endurance Cycling testing as described in Section 3.1, the devices under test shall be programmed with a checkerboard pattern (i.e., where each bit is surrounded by its complement). In some cases, an alternative pattern such as a logical checkerboard may better represent a worst-case condition. Alternative patterns are acceptable when agreed to by user and supplier. With user acceptance, data may also be written using a mode of programming that is different from that specified in the datasheet, to modify the margins of the cells and obtain additional acceleration. For multi-level-cell (MLC) memories, the pattern must include all possible combinations of cell + cell nearest neighbor combinations.

b. Devices with embedded and stand-alone NVM shall be subjected to High Temperature Operating Life (HTOL) testing per Table 2 of AEC-Q100, using temperature and duration conditions meeting or exceeding the HTOL requirement for the device specified operating temperature grade. During this test, all addresses in the NVM array shall be accessed (read) to the maximum possible number of reads (per AEC-Q100 test B3) without impacting the HTOL exercise of the Logic (per AEC-Q100 test B1). Otherwise, separate HTOL tests shall be performed for the NVM and Logic memory blocks. For the duration of the test, full memory array checksum (i.e., "Bit Flip") testing must be continuously performed at speed for embedded flash microprocessors. The stand-alone flash (discrete) could be exempt from this checksum requirement upon supplier-customer agreement.

c. Only data pattern verification and non-array altering functional testing is performed at interim read points. This purposely excludes any program or erase testing of the NVM array.

d. At the qualification point, devices are first tested to verify that the data pattern has been retained at temperature(s) justified by the supplier. This is to be followed by full functional testing to the device specification, per AEC-Q100 test B1. At this point, full functional testing consists of array altering program and erase events.

e. If the supplier demonstrates that the stress duration of HTOL for the selected device grade is longer than the respective HTDR stress duration, with user acceptance, the supplier may derate the HTOL period of cycled bits. In the latter case, recoverable (soft) bit data errors occurring during HTOL testing at times beyond the equivalent HTDR life period will not be counted towards HTOL failures but rather as HTDR failures at time points exceeding the qualification stress time requirement.

3.5 Test Precautions

Precautions shall be taken to ensure that devices cannot be damaged by thermal runaway of the device or tester and to preclude electrical damage. The test setup shall be monitored initially and at the conclusion of a test interval to establish that all devices are being stressed to the specified requirements. The bias voltages and currents on each device shall be noted and corrected prior to further temperature exposure. If a device is not biased properly when checked at the conclusion of a test interval, it must be determined if the device has changed or if the test circuit has changed so that the validity of the data for qualification can be established.

3.6 Measurements

3.6.1 Electrical Measurements

The electrical measurements shall be made at intervals per the applicable device specification. Interim and final electrical measurements shall be completed within 96 hours after removal of the devices from the specified test conditions.

3.6.2 Required Measurements

The electrical measurements shall consist of parametric and functional tests specified in the applicable device specification.

3.6.3 Measurement Conditions

Before removing the devices from the chamber, the ambient temperature shall be returned to room temperature while maintaining the specified voltages on the devices. Testing shall be conducted at typical conditions and at minimum and maximum of temperature range per part specification and according to the respective part grade listed in AEC-Q100 Section 1.3.3.

4. FAILURE CRITERIA

A device will be defined as a failure if the parametric limits are exceeded, the device no longer meets the device specification requirements, or the device fails to retain its intended data state.

During Program/Erase Endurance Cycling testing, failure occurs when a write or erase event is not completed in less than the maximum specified time or when the event completes but the data pattern within the memory array does not correspond to the intended data pattern.

5. SUMMARY

The following details shall be included in the supplier's stress test specification or the applicable device specification:

a. Special mounting, if applicable.
b. Test condition, alphanumeric code.
c. Biasing conditions.
d. Measurements before, at intermediate test points (if applicable), and after test.
e. Maximum number of logic transitions in the memory cell.
f. Period between program/erase cycles.
g. Cycling temperature and total cycling duration at temperature.
h. Segmentation of the device to cycling blocks, and the total number of cycles of each block-segment.
i. Alternative procedures requested by the NVM supplier, including but not limited to program/erase cycle sequencing, separate samplings for the test sequence described in Figure 1, data retention duration and temperature, and checksum testing on stand-alone NVM devices, must be approved by the user.

Appendix A: Calculating High Temperature Endurance Stress Time

Let us assume product target lifetime is 15 years. Let us assume worst case (fastest) cycling frequency is total Program/Erase cycling specification exercised over the first 3 years only (the lower the worst for annealing cycling-induced damage). Let us assume that worst case use temperature during cycling and in between cycles is T_U = 55°C (the lower the worst for annealing cycling-induced damage). Let us assume that the devices under test are silicon/tunnel-oxide/floating gate devices with charge-detrapping activation energy of E_{aa} = 1.1 eV for healing oxide defects (JEDEC publication JEP122D Ch. 5.5; value may be product specific, and must be justified/demonstrated by supplier). Let us assume the selected cycling temperature is 90°C.

The cycling/detrapping thermal acceleration factor for cycling stress at T_S = 90°C is

$$TAF_{cycling} = exp[E_{aa}/k_B(1/(273+T_U) - 1/(273+T_S))] = 42.6$$

where k_B is Boltzmann constant = 0.00008617 eV/K.

The maximum allowed cycling duration at 90°C is

3 [yr] x 8760 [h/yr] / 42.6 = 616 h

with cycling distributed evenly over the allowed cycling period at the elevated temperature.

Appendix B: Equivalent Bake Time Examples

Equivalent bake times are calculated according to $t_u = t \cdot exp[E_{aa}/k_B(1/T_s - 1/T_u)]$, where t is the application use time at temperature T, t_u is the stress time at temperature T_s, and k_B = 0.00008617 eV/K

Table B1: HTDR Equivalent Bake Time for Selected Mission Profile for Eaa = 1.1 eV

	Temp [°C]	Use Time [h]	Eq. time @ 150°C	Eq. time @ 175°C
Operation	150	100	100.0	18.6
Operation	120	900	89.9	16.7
Operation	110	5000	213.9	39.7
Operation	90	6000	40.5	7.6
	Total Op:	12000	445	83
Non-op	90	1000	6.8	1.3
Non-op	40	118400	1.9	0.4
	Total Non-Op:	119400	9	2
	Total [h]:	**131400**	**453**	**84**

Table B2: HTSL Equivalent Bake Time for Above Mission Profile for Eaa = 0.60 eV

	Temp [°C]	Use Time [h]	Eq. time @ 150°C	Eq. time @ 175°C
Operation	150	100	100.0	39.9
Operation	120	900	256.2	102.2
Operation	110	5000	896.1	357.6
Operation	90	6000	394.9	157.6
	Total Op:	12000	1647	657
Non-op	90	1000	65.8	26.3
Non-op	40	118400	287.0	114.5
	Total Non-Op:	119400	353	141
	Total [h]:	**131400**	**2000**	**798**

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release
A	May 19, 1995	Merged 005 and 006 into single spec.
B	July 18, 2003	Complete revision. Title change to NONVOLATILE MEMORY PROGRAM/ERASE ENDURANCE, DATA RETENTION, AND OPERATIONAL LIFE TEST. All references to EEPROM replaced with Nonvolatile Memory. Added new Figure 1. New section 3.3 added for Operational Life testing.
C	Sept. 7, 2004	Complete revision.
D	Oct. 11, 2011	Complete revision. Revised Acknowledgment; Change Notification; Sections 1, 3, 3.1, 3.2, 3.3, 3.4, 3.5, 3.5.1, 3.5.2, 3.5.3, 4, and 5; and Figure 1. Added New Section 3.3, Appendix A, Appendix B, and Figure 2.
D1	Jan. 9, 2012	Corrected errors that occurred during publication of Q100-005D. Revised Sections 1, 3.1, 3.3, Figure 2, Appendix A, and Appendix B. Added NEW Table B1 and B2 captions.