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# FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR INTEGRATED CIRCUITS



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- AEC-Q100-001: WIRE BOND SHEAR TEST
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# **Revision Summary**

This informative section briefly describes the changes made in the AEC-Q100 Rev-H document, compared to previous document version, AEC-Q100 Rev-G (May 14, 2007). Punctuation and text improvements are not included in this summary.

- Section 1.2.1 Automotive Reference Documents: Added reference to AEC-Q005 Pb-Free Requirements
- NEW Section 1.2.4 Decommissioned Reference Documents: Added new section providing guidance on elimination of AEC-Q100-003 Machine Model ESD (removed due to industry test obsolescence) and Q100-006 Electrothermally Induced Gate Leakage (removed due to lack of industry need as a qualification test)
- Section 1.3.1 AEC Q100 Qualification: Added recommendation that passing ESD voltage level be specified in supplier datasheet with footnote on any pin exceptions
- NEW Section 1.3.2 AEC Certification: Added new definition clarifying that AEC-Q100 "certification" does not exist, suppliers perform qualification testing according to AEC standards
- Section 1.3.4 Definition of Part Operating Temperature Grade: Added new Table 1 defining part operating temperature grades and guidance on use of temperature (e.g., endpoint, junction) during tests; eliminated Grade 4 (0°C to +70°C) entry
- NEW Section 1.3.5 Capability Measure, Cpk: Added new definition and reference to AEC-Q003
   Characterization document
- Section 2.2 Precedence of Requirements: Added clarification to Purchase Order and Device Specification entries
- Section 2.3.1 Definition of Generic Data: Moved existing Table 1, Part Qualification/Requalification Lot Requirements, and portion of section text to Appendix 1 Definition of a Product Qualification Family
- Section 2.3.2 Time Limit for Acceptance of Generic Data: Added text on use of diagram in Figure 1
- Section 2.4.1 Lot Requirements: Added statement that deviation from Table 2 requires technical explanation
- Section 2.5 Definition of Test Failure After Stressing: Added statement on EOS
- Section 3.1.1 Qualification of A New Device Manufactured in A Currently Qualified Family: Deleted this entire section, subject is covered in Appendix 1.
- Section 3.2.3 Criteria for Passing Requalification: Modified text to provide better guidance on AEC-Q100 requalification
- NEW Section 3.3 Qualification of A Pb-Free Device: Added new section with requirements for Pb-Free devices and references to AEC-Q005 Pb-Free Requirements document
- Figure 2 Qualification Test Flow:
  - Test Group A: Removed statement of PC before PTC
  - Test Group B: Corrected test temperature order for post-HTOL testing to Room, Cold, & Hot
  - Test Group E: Removed reference to MM ESD and GL tests
- Table 2 Qualification Test Methods:
  - Test A3 Autoclave or Unbiased HAST or Temperature Humidity (without Bias): Added TH reference to Additional Requirements column
  - Test A4 Temperature Cycling: Revised low-end temperature and minimum duration; added legacy test temperature note; eliminated Grade 4 entry
  - Test A6 High Temperature Storage Life: Added reference to Ta (ambient temperature)
  - Test A7 High Temperature Operating Life: Removed 408 hour test duration option; added notes regarding use of Ta (ambient temperature) and Tj (junction temperature)
  - Test C1 Wire Bond Shear: Removed Ppk requirement; modified Cpk accept criteria to Cpk>1.67; added reference to AEC-Q003
  - Test C2 Wire Bond Pull: Removed Ppk requirement; modified Cpk accept criteria to
  - Cpk>1.67; added reference to AEC-Q003
  - o Test C3 Solderability: Added reference to J-STD-002D and statement on use of dry bake

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# **Revision Summary (continued)**

- Table 2 Qualification Test Methods (continued):
  - Test C4 Physical Dimension: Removed Ppk requirement; modified Cpk accept criteria to Cpk>1.67; added reference to AEC-Q003
  - Test C5 Solder Ball Shear: Removed Ppk requirement; modified Cpk accept criteria to Cpk>1.67; added reference to AEC-Q003
  - Test E2 Electrostatic Discharge Human Body Model/Machine Model: Eliminated Machine Model (MM) ESD entry; added reference to Section 1.3.1
  - Test E3 Electrostatic Discharge Charged Device Model: Added reference to Section 1.3.1
  - Test E5 Electrical Distribution: Added Cpk>1.67 accept criteria and reference to AEC-Q003
  - Eliminated Test E8 Electrothermally Induced Gate Leakage entry
  - NEW Test E12 Lead (Pb) Free: Added new test entry
  - Test F1 Part Average Testing: Modified Additional Requirements providing guidance on sample sizes and accept criteria
  - Test F2 Statistical Bin/Yield Analysis: Modified Additional Requirements providing guidance on sample sizes and accept criteria
  - Test G1 Mechanical Shock: Modified sample size/lot and number of lots
  - Test G2 Variable Frequency Vibration: Modified sample size/lot and number of lots
  - Test G3 Constant Acceleration: Modified sample size/lot and number of lots
  - Test G4 Gross/Fine Leak: Modified sample size/lot and number of lots
  - Test G8 Internal Water Vapor: Modified sample size/lot
  - Table 2 Legend: Added Note L reference for Pb-Free devices
- Table 3 Process Change Qualification Guidelines for the Selection of Tests: Removed MM (Machine Model) ESD and GL (Gate Leakage) entries; added LF (Lead Free) entry
- Appendix 1 Definition of a Product Qualification Family: Complete revision
  - NEW Section A1.1 Product: Added new section and text
  - NEW Section A1.4 Qualification/Requalification Lot Requirements: Relocated original AEC-Q100 Rev G Table 1 to Appendix 1 and renumbered as Table A1.1
  - Revised Table A1.1 Part Qualification/Requalification Lot Requirements: Deleted row titled "A new part that has some applicable generic data"; added NEW entry where "The part to be qualified is slightly more complex"
  - NEW Table A1.2 Examples for Generic Data Use: Added new Table and content
- Appendix Template 4A AEC-Q100 Qualification Test Plan:
  - Test C3, SD Solderability: Added reference to J-STD-002D and requirement of steam aging
  - Test E2, HBM/MM ESD Human Body/machine Model: Eliminated MM entry
  - Test E8, GL Electrothermally Induced Gate Leakage: Eliminated GL entry
  - o Tests G1-G4, MECH Hermetic Package Tests: Modified sample size and lot requirements
- Appendix Template 4B AEC-Q100 Generic Data:
  - Test C3, SD: Added reference to J-STD-002D and requirement of steam aging
  - Test E2, HBM/MM: Eliminated MM entry
  - o Test E8, GL: Eliminated GL entry
  - Test G1, MS: Modified sample size and lot requirements
  - Test G2, VFV: Modified sample size and lot requirements
  - Test G3, CA: Modified sample size and lot requirements
  - Test G4, GFL: Modified sample size and lot requirements
  - Complete revision of Generic Data Part Attributes Section
- NEW Appendix 7 Guideline on Relationship of Robustness Validation to AEC-Q100: Added NEW Section and text, including NEW Figures A7.1 & A7.2 and NEW Table A7.1



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# FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR PACKAGED INTEGRATED CIRCUITS

Text enhancements and differences made since the last revision of this document are shown as underlined areas. Several figures and tables have also been revised, but changes to these areas have not been underlined.

# <u>Unless otherwise stated herein, the date of implementation of this standard for new gualifications and re-qualifications is as of the publish date above.</u>

## 1. SCOPE

This document contains a set of failure mechanism based stress tests and defines the minimum stress test driven qualification requirements and references test conditions for qualification of integrated circuits (ICs). These tests are capable of stimulating and precipitating semiconductor device and package failures. The objective is to precipitate failures in an accelerated manner compared to use conditions. This set of tests should not be used indiscriminately. Each qualification project should be examined for:

- a. Any potential new and unique failure mechanisms.
- b. Any situation where these tests/conditions may induce failures that would not be seen in the application.
- c. Any extreme use condition and/or application that could adversely reduce the acceleration.

Use of this document does not relieve the IC supplier of their responsibility to meet their own company's internal qualification program. In this document, "user" is defined as all customers using a device qualified per this specification. The user is responsible to confirm and validate all qualification data that substantiates conformance to this document. Supplier usage of the device temperature grades as stated in this specification in their part information is strongly encouraged.

#### 1.1 Purpose

The purpose of this specification is to determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality/reliability in the application.

## 1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

## 1.2.1 Automotive

AEC-Q001 Guidelines for Part Average Testing AEC-Q002 Guidelines for Statistical Yield Analysis AEC-Q003 Guidelines for Characterizing the Electrical Performance AEC-Q004 Zero Defects Guideline (DRAFT) <u>AEC-Q005 Pb-Free Requirements</u> SAE J1752/3 Integrated Circuits Radiated Emissions Measurement Procedure

## 1.2.2 Military

MIL-STD-883 Test Methods and Procedures for Microelectronics

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## 1.2.3 Industrial

JEDEC JESD-22 Reliability Test Methods for Packaged Devices UL-STD-94 Tests for Flammability of Plastic materials for parts in Devices and Appliances IPC/JEDEC J-STD-020 Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices JESD89 Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices JESD89-1 System Soft Error Rate (SSER) Test Method JESD89-2 Test Method For Alpha Source Accelerated Soft Error Rate JESD89-3 Test Method for Beam Accelerated Soft Error Rate

## 1.2.4 Decommissioned

AEC Q100-003 ESD Machine Model

• <u>Removed from JEDEC due to obsolescence. HBM and CDM cover virtually all known</u> <u>ESD-related failure mechanisms.</u>

AEC Q100-006 Electrothermally-Induced Gate Leakage

• Removed due to the lack of need for it as a qualification test.

### 1.3 Definitions

#### 1.3.1 AEC Q100 Qualification



## 1.3.2 AEC Certification

Note that there are no "certifications" for AEC-Q100 qualification and there is no certification board run by AEC to qualify parts. Each supplier performs their qualification to AEC standards, considers customer requirements and submits the data to the customer to verify compliance to Q100.

#### 1.3.<u>3</u> Approval for Use in an Application

"Approval" is defined as user approval for use of a part in their application. The user's method of approval is beyond the scope of this document.

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## 1.3.4 Definition of Part Operating Temperature Grade

The part operating temperature grades are defined in Table 1 below:

## Table 1: Part Operating Temperature Grades

<u>Grade</u>	Ambient Operating Temperature Range
<u>o</u>	<u>-40°C to +150°C</u>
1	<u>-40°C to +125°C</u>
<u>2</u>	<u>-40°C to +105°C</u>
<u>3</u>	<u>-40°C to +85°C</u>

The endpoint test temperatures for hot and cold test, if required for that stress test, must be equivalent to those specified for the particular grade. If accounting for junction heating during powered test, hot test endpoint test temperature can be greater.

For Test Group B – Accelerated Lifetime Simulation Tests: High Temperature Operating Life (HTOL), Early Life Failure Rate (ELFR) and NVM Endurance, Data Retention, and Operational Life (EDR), the junction temperature of the device during stressing should be equal to or greater than the hot temperature for that grade.

#### 1.3.5 Capability Measures Cpk

Refer to AEC-Q003 Characterization to understand how the Cpk measure will be used in this standard.

## 2. GENERAL REQUIREMENTS

#### 2.1 Objective

The objective of this specification is to establish a standard that defines operating temperature grades for integrated circuits based on a minimum set of qualification requirements.

#### 2.1.1 Zero Defects

Qualification and some other aspects of this document are a subset of, and contribute to, the achievement of the goal of Zero Defects. Elements needed to implement a zero defects program can be found in AEC-Q004 Zero Defects Guideline.

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## 2.2 Precedence of Requirements

In the event of conflict in the requirements of this standard and those of any other documents, the following order of precedence applies:

- a. The purchase order (or master purchase agreement terms and conditions)
- b. The (mutually agreed) individual device specification
- c. This document
- d. The reference documents in Section 1.2 of this document
- e. The supplier's data sheet

For the device to be considered a qualified part per this specification, the purchase order and/or the individual device specification cannot waive or detract from the requirements of this document.

## 2.3 Use of Generic Data to Satisfy Qualification and Requalification Requirements

#### 2.3.1 Definition of Generic Data

The use of generic data to simplify the qualification process is strongly encouraged. Generic data can be submitted to the user as soon as it becomes available to determine the need for any additional testing. To be considered, the generic data must be based on a matrix of specific requirements associated with each characteristic of the device and manufacturing process as shown in Table 3 and Appendix 1. If the generic data contains any failures, the data is not usable as generic data unless the supplier has documented and implemented corrective action or containment for the failure condition that is acceptable to the user.

Appendix 1 defines the criteria by which components are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable for the qualification of the device in question. For each stress test, two or more qualification families can be combined if the reasoning is technically sound (i.e., supported by data).

Table 3 defines a set of qualification tests that must be considered for any changes proposed for the component. The Table 3 matrix is the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and user should use as a baseline for discussion of tests that are required for the qualification in question. It is the supplier's responsibility to present rationale for why any of the recommended tests need not be performed.

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## 2.3.3 Time Limit for Acceptance of Generic Data

There are no time limits for the acceptability of generic data. <u>Use the diagram below for appropriate</u> <u>sources of reliability data that can be used</u>. This data must come from the specific part or a part in the same qualification family, as defined in Appendix 1. <u>Potential sources of data could</u> include any customer specific data (withhold customer name), process change qualification, and periodic reliability monitor data (see Figure 1).



**Note:** Some process changes (e.g., die shrink) will affect the use of generic data such that data obtained before these types of changes will not be acceptable for use as generic data.

## Figure 1: Generic Data Time Line

## 2.4 Test Samples

#### 2.4.1 Lot Requirements

Test samples shall consist of a representative device from the qualification family. Where multiple lot testing is required due to a lack of generic data, test samples as indicated in Table 2 must be composed of approximately equal numbers from non-consecutive wafer lots, assembled in non-consecutive molding lots. That is, they must be separated in the fab or assembly process line by at least one non-qualification lot. Any deviation from the above requires technical explanation from the supplier.

## 2.4.2 Production Requirements

All qualification devices shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at production volumes. Other electrical test sites may be used for electrical measurements after their electrical quality is validated.

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### 2.4.3 Reusability of Test Samples

Devices that have been used for nondestructive qualification tests may be used to populate other qualification tests. Devices that have been used for destructive qualification tests may not be used any further except for engineering analysis.

### 2.4.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 2.

If the supplier elects to use generic data for qualification, the specific test conditions and results must be recorded and available to the user (preferably in the format shown in Appendix 4). Existing applicable generic data should first be used to satisfy these requirements and those of <u>Section 2.3</u> for each test requirement in Table 2. Device specific qualification testing should be performed if the generic data does not satisfy these requirements.

#### 2.4.5 Pre- and Post-stress Test Requirements

End-point test temperatures (room, hot and/or cold) are specified in the "Additional Requirements" column of Table 2 for each test.

## 2.5 Definition of Test Failure After Stressing

Test failures are defined as those devices not meeting the individual device specification, criteria specific to the test, or the supplier's data sheet, in the order of significance as defined in Section 2.2. Any device that shows external physical damage attributable to the environmental test is also considered a failed device. If the cause of failure is due to mishandling <u>during stressing or testing</u> <u>such as EOS or</u> ESD, or some other cause unrelated to the <u>component reliability</u>, the failure shall be discounted but reported as part of the data submission.

## 3. QUALIFICATION AND REQUALIFICATION

#### 3.1 Qualification of a New Device

The stress test requirement flow for qualification of a new device is shown in Figure 2 with the corresponding test conditions defined in Table 2. For each qualification, the supplier must have data available for all of these tests, whether it is stress test results on the device to be qualified or acceptable generic data. A review shall also be made of other devices in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the user.

For each device qualification, the supplier must have available the following:

- Certificate of Design, Construction and Qualification (see Appendix 2)
- Stress Test Qualification data (see Table 2 & Appendix 4)
- Data indicating the level of fault grading of the software used for qualification (when applicable to the device type) per Q100-007 that will be made available to the customer upon request

## 3.2 Requalification of a Changed Device

Requalification of a device is required when the supplier makes a change to the product and/or process that impacts (or could potentially impact) the form, fit, function, quality and/or reliability of the device (see Table 3 for guidelines).

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### 3.2.1 Process Change Notification

The supplier will meet the user requirements for product/process changes.

#### 3.2.2 Changes Requiring Requalification

As a minimum, any change to the product, as defined in Appendix 1, requires performing the applicable tests listed in Table 2, using Table 3 to determine the requalification test plan. Table 3 should be used as a guide for determining which tests are applicable to the qualification of a particular part change or whether equivalent generic data can be submitted for that test(s).

## 3.2.3 Criteria for Passing Requalification

All requalification failures shall be analyzed for root cause. <u>Only when</u> corrective and preventative actions are in place, the part may then be considered AEC Q100 qualified again.

#### 3.2.4 User Approval

A change may not affect a device's operating temperature grade, but may affect its performance in an application. Individual user authorization of a process change will be required for that user's particular application(s), and this method of authorization is outside the scope of this document.

#### 3.3 Qualification of a Pb-Free Device

Added requirements needed to address the special quality and reliability issues that arise when Lead (Pb)-Free processing is utilized is specified in AEC-Q005 Pb-Free Requirements. Materials used in Pb-Free processing include the termination plating and the board attach (solder). These new materials usually require higher board attach temperatures to yield acceptable solder joint quality and reliability. These higher temperatures may adversely affect the moisture sensitivity level of plastic packaged semiconductors. As a result, new, more robust mold compounds may be required. If an encapsulation material change is required to provide adequate robustness for Pb-Free processing of the device, the supplier should refer to the process change qualification requirements in this specification. Preconditioning should be performed at the Pb-free reflow classification temperatures described in IPC/JEDEC J-STD-020 Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices before environmental stress tests.

#### 4. QUALIFICATION TESTS

#### 4.1 General Tests

Test flows are shown in Figure 2 and test details are given in Table 2. Not all tests apply to all devices. For example, certain tests apply only to ceramic packaged devices, others apply only to devices with NVM, and so on. The applicable tests for the particular device type are indicated in the "Note" column of Table 2. The "Additional Requirements" column of Table 2 also serves to highlight test requirements that supersede those described in the referenced test method. Any unique qualification tests or conditions requested by the user and not specified in this document shall be negotiated between the supplier and user requesting the test.

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## 4.2 Device Specific Tests

The following tests must be performed on the specific device to be qualified for all hermetic and plastic packaged devices. Generic data is not allowed for these tests. Device specific data, if it already exists, is acceptable.

- 1. Electrostatic Discharge (ESD) All product.
- 2. Latch-up (LU) All product.
- 3. Electrical Distribution The supplier must demonstrate, over the operating temperature grade, voltage, and frequency, that the device is capable of meeting the parametric limits of the device specification. This data must be taken from at least three lots, or one matrixed (or skewed) process lot, and must represent enough samples to be statistically valid, see Q100-009. It is strongly recommended that the final test limits be established using AEC-Q001 Guidelines For Part Average Testing.
- 4. Other Tests A user may require other tests in lieu of generic data based on his experience with a particular supplier.

#### 4.3 Wearout Reliability Tests

Testing for the failure mechanisms listed below must be available to the user whenever a new technology or material relevant to the appropriate wearout failure mechanism is to be qualified. The data, test method, calculations, and internal criteria need not be demonstrated or performed on the qualification of every new device, but should be available to the user upon request.

- Electromigration
- Time-Dependent Dielectric Breakdown (or Gate Oxide Integrity Test) for all MOS technologies
- Hot Carrier Injection for all MOS technologies below 1 micron
- Negative Bias Temperature Instability
- Stress Migration

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Figure 2: Qualification Test Flow

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	TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS														
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS							
Preconditioning	PC	A1	P, B, S, N, G	77	3	0 Fails	JEDEC J-STD-020 JESD22-A113	Performed on surface mount devices only. PC performed before THB/HAST, AC/UHST, TC, and PTC stresses. It is recommended that J-STD-020 be performed to determine what preconditioning level to perform in the actual PC stress per JA113. The minimum acceptable level for qualification is level 3 per JA113. Where applicable, preconditioning level and Peak Reflow Temperature must be reported when preconditioning and/or MSL is performed. Delamination from the die surface in JA113/J- STD-020 is acceptable if the device passes the subsequent Qualification tests. Any replacement of devices must be reported. <b>TEST before and after PC at</b> <b>room temperature</b> .							
Temperature- Humidity-Bias or Biased HAST	THB or HAST	A2	P, B, D, G	77	3	0 Fails	JEDEC JESD22-A101 or A110	For surface mount devices, PC before THB (85°C/85%RH for 1000 hours) or HAST (130°C/85%RH for 96 hours, or 110°C/85%RH for 264 hours). <b>TEST before and after</b> <b>THB or HAST at room and hot temperature.</b>							
Autoclave or Unbiased HAST or Temperature- Humidity (without Bias)	AC or UHST or TH	A3	P, B, D, G	77	3	0 Fails	JEDEC JESD22-A102, A118, or A101	For surface mount devices, PC before AC (121°C/15psig for 96 hours) or unbiased HAST (130°C/85%RH for 96 hours, or 110°C/85%RH for 264 hours). For packages sensitive to high temperatures and pressure (e.g., BGA), PC followed by TH (85°C/85%RH) for 1000 hours may be substituted. <b>TEST before and after AC, UHST<u>, or TH</u> at room temperature.</b>							

## Table 2: Qualification Test Methods

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		TEST	GROU	P A – A	CCELERA	TED ENV	IRONMEN	NT STRESS 1	ESTS (CONTINUED)				
	STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS				
1.CC	Temperature Cycling 0m 139171656	тс	A4	H, P, B, D, G	77	3	0 Fails	JEDEC JESD22-A104 and Appendix 3	<ul> <li>PC before TC for surface mount devices.</li> <li>Grade 0: <u>-55°C</u> to +150°C for 2000 cycles <u>or equivalent</u>.</li> <li>Grade 1: <u>-55°C</u> to +150°C for 1000 cycles <u>or equivalent</u>.</li> <li>Note: <u>-65°C</u> to 150°C for 500 cycles is also an allowed test condition due to legacy use with no known lifetime issues.</li> <li>Grade 2: <u>-55°C</u> to +125°C for 1000 cycles <u>or equivalent</u>.</li> <li>Grade 3: <u>-55°C</u> to +125°C for 500 cycles <u>or equivalent</u>.</li> <li>TEST before and after TC at hot temperature. After completion of TC, decap five devices from one lot and perform WBP (test #C2) on corner bonds (2 bonds per corner) and one mid-bond per side <i>on each device</i>.</li> <li>Preferred decap procedure to minimize damage and chance of false data is shown in Appendix 3.</li> </ul>				
	Power Temperature Cycling	PTC	A5	H, P, B, D, G 45 1		1	0 <u>Fails</u>	JEDEC JESD22-A105	PC before PTC for surface mount devices. Test required only on devices with maximum rated power ≥ 1 watt or $\Delta T_J \ge$ 40°C or devices designed to drive inductive loads. <b>Grade 0:</b> T <sub>a</sub> of -40°C to +150°C for 1000 cycles. <b>Grade 1:</b> T <sub>a</sub> of -40°C to +125°C for 1000 cycles. <b>Grades 2</b> and 3: T <sub>a</sub> -40°C to +105°C for 1000 cycles. Thermal shut-down shall not occur during this test. <b>TEST</b> <b>before and after PTC at room and hot temperature.</b>				
	High Temperature Storage Life	HTSL	A6	H, P, B, D, G, K	45	1	0 <u>Fails</u>	JEDEC JESD22-A103	Plastic Packaged Parts Grade 0: $+175^{\circ}$ C $\underline{T}_a$ for 1000 hours or $+150^{\circ}$ C $\underline{T}_a$ for 2000 hours.Grade 1: $+150^{\circ}$ C $\underline{T}_a$ for 1000 hours or $+175^{\circ}$ C $\underline{T}_a$ for 500 hours.Grades 2 and 3: $+125^{\circ}$ C $\underline{T}_a$ for 1000 hours or $+150^{\circ}$ C $\underline{T}_a$ for 500 hours.Ceramic Packaged Parts $+250^{\circ}$ C $\underline{T}_a$ for 10 hours or $+200^{\circ}$ C $\underline{T}_a$ for 72 hours.TEST before and after HTSL at room and hot temperature.* NOTE: Data from Test B3 (EDR) can be substituted for Test A6 (HTSL) if package and grade level requirements are met.				

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			TEST	ME SIMULATION TESTS							
	STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS		
sh.co	High Temperature Operating Life 6567	HTOL	B1	H, P, B, D, G, K	77	3	0 <u>Fails</u>	JEDEC JESD22-A108	<ul> <li>For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005.</li> <li>Grade 0: +150°C T<sub>a</sub> for 1000 hours.</li> <li>Grade 1: +125°C T<sub>a</sub> for 1000 hours.</li> <li>Grade 2: +105°C T<sub>a</sub> for 1000 hours.</li> <li>Grade 3: +85°C T<sub>a</sub> for 1000 hours.</li> <li>HTOL NOTES: <ol> <li>HTOL stress times for the appropriate grade Ta are the min requirement; the Tj of the test (measured or calculated) should be available.</li> <li>Tj may be used instead of Ta when performing HTOL provided that Tj of the device under HTOL conditions is equal to or higher than the Tj maximum operating (Tjopmax) of the particular device, but below the absolute maximum Tj.</li> <li>If Tj is used to set the HTOL conditions, the minimum stress of 1000 hours at the Ta of the device is to be shown using activation energy of 0.7ev or other value technically justified.</li> <li>V<sub>cc</sub> (max) at which dc and ac parametrics are guaranteed. Thermal shut-down shall not occur during this test. TEST before and after HTOL at room, cold. and hot temperature (in that order).</li> </ol> </li> </ul>		
	Early Life Failure Rate	ELFR	B2	H, P, B, N, G	800	3	0 <u>Fails</u>	AEC Q100-008	Devices that pass this stress can be used to populate other stress tests. Generic data is applicable. <b>TEST before and after ELFR at room and hot temperature.</b>		
	NVM Endurance, Data Retention, and Operational Life	EDR	B3	H, P, B, D, G, K	77	3	0 <u>Fails</u>	AEC Q100-005	TEST before and after EDR at room and hot temperature. Sample size and lot requirement applies to EACH of the NVM tests per Q100-005.		

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	TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS														
	STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS						
	Wire Bond Shear	WBS	C1	H, P, D, G		R.V	<u>С<sub>РК</sub> &gt;1.67</u>	AEC Q100-001 <u>AEC Q003</u>	At appropriate time interval for each bonder to be used.						
	Wire Bond Pull	WBP	C2	H, P, D, G	30 bonds fror of 5 de	n a minimum evices	<u>C<sub>PK</sub> &gt;1.67</u> or 0 Fails after TC (test #A4)	MIL-STD883 Method 2011 <u>AEC Q003</u>	Condition C or D. For Au wire diameter ≥1mil, minimum pull strength after TC = 3 grams. For Au wire diameter <1mil, refer to Figure 2011-1 in MIL-STD-883 Method 2011 as a guideline for minimum pull strength. For Au wire diameter <1mil, wire bond pull shall be performed with the hook over the ball bond and not at mid-wire.						
eice-sh.coi	Solderability n 1391716567	SD	C3	H, P, D, G	15	1	>95% lead coverage	JEDEC JESD22-B102 <u>JEDEC</u> J <u>-STD-002D</u>	If burn-in screening is normally performed on the device before shipment, samples for SD must first undergo burn-in. Perform 8 hour steam aging prior to testing (1 hour for Au-plated leads). The customer can request justification for using dry bake in place of steam aging.						
	Physical Dimensions	PD		H, P, D, G	10	3	<u>С<sub>РК</sub> &gt;1.67</u>	JEDEC JESD22-B100 and B108 <u>AEC Q003</u>	See applicable JEDEC standard outline and individual device spec for significant dimensions and tolerances.						
	Solder Ball Shear	Solder Ball Shear SBS			5 balls from a min. of 10 devices	3	<u>С<sub>РК</sub> &gt;1.67</u>	AEC Q100-010 <u>AEC Q003</u>	PC thermally (two 220°C reflow cycles) before integrity (mechanical) testing. <u>Refer to J-STD- 020 for Pb-free reflow profiles to be used for this</u> test.						
	Lead Integrity	LI	C6	H, P, D, G	10 leads from each of 5 parts	1	No lead breakage or cracks	JEDEC JESD22-B105	Not required for surface mount devices. Only required for through-hole devices.						
			TES	ST GRO	UP D – DII	E FABRIC	ATION RELI	ABILITY TES	TS						
	STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS						
	Electromigration	EM	D1						The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.						
	Time Dependent Dielectric Breakdown	TDDB	D2						The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.						

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## Table 2: Qualification Test Methods (continued)

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS (CONTINUED)													
STRESS	STRESS     ABV     #     NOTES     SAMPLE SIZE / LOT     NUMBER OF LOTS     ACCEPT CRITERIA     TEST METHOD     ADDITIONAL REQUIREMENT												
Hot Carrier Injection	НСІ	D3						The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.					
Negative Bias Temperature Instability	NBTI	D4	>					The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.					
Stress Migration	SM	D5	X	<u> </u>				The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.					

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## **TEST GROUP E – ELECTRICAL VERIFICATION TESTS**

STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Pre- and Post-Stress Function/Parameter	TEST	E1	H, P, B, N, G	All	All	0 <u>F</u> ails	Test program to supplier data sheet or user specification	Test is performed as specified in the applicable stress reference and the additional requirements in Table 2 and illustrated in Figure 2. Test software used shall meet the requirements of Q100-007. All electrical testing before and after the qualification stresses are performed to the limits of the individual device specification in temperature and limit value.
Electrostatic Discharge Human Body Model	НВМ	E2	H, P, B, D	See Test Method	1	Target: 0 Fails 2KV HBM ( <u>Classification 2</u> or better)	AEC Q100-002	<b>TEST before and after ESD at room and hot temperature</b> . Device shall be classified according to the maximum withstand voltage level. Device levels <2000V HBM require specific user approval. <u>Refer to Section 1.3.1.</u>
Electrostatic Discharge Charged Device Model	CDM	E3	H, P, B, D	See Test Method	1	Target: 0 Fails 750V corner pins, 500V all other pins ( <u>Classification</u> C <u>4B</u> or better)	AEC Q100-011	<b>TEST before and after ESD at room and hot</b> <b>temperature</b> . Device shall be classified according to the maximum withstand voltage level. Device levels <750V corner pins and/or <500V all other pins CDM require specific user approval. <u>Refer to Section 1.3.1.</u>

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TEST GROUP E – ELECTRICAL VERIFICATION TESTS (CONTINUED)													
STRESS	ABV	#	TEST METHOD	ADDITIONAL REQUIREMENTS									
Latch-Up	LU E4 <sup>H, P, B,</sup> 6 1 0 Fail					0 Fails	AEC Q100-004	See attached procedure for details on how to perform the test. <b>TEST before and after LU at room and hot temperature.</b>					
Electrical Distributions	ons ED		H, P, B, D	30	3	<u>Where</u> applicable, <u>C<sub>PK</sub> &gt;1.67</u>	AEC Q100-009 <u>AEC Q003</u>	Supplier and user to mutually agree upon electrical parameters to be measured and accept criteria. <b>TEST at room, hot, and cold</b> <b>temperature.</b>					
Fault Grading	FG	E6	X			AEC Q100-007 unless otherwise specified	AEC Q100-007	For production testing, see Q100-007 for test requirements.					
Characterization 67	CHAR	E7	<b>&gt;</b>				AEC Q003	To be performed on new technologies and part families.					
Electromagnetic Compatibility	EMC	E9		1	1		SAE J1752/3 – Radiated Emissions	See Appendix 5 for guidelines on determining the applicability of this test to the device to be qualified. This test and its accept criteria is performed per agreement between user and supplier on a case-by-case basis.					
Short Circuit Characterization	SC	E10	D, G	10	3	0 Fails	AEC Q100-012	Applicable to all smart power devices. This test and statistical evaluation (see <u>Section 4 of Q100-012</u> ) shall be performed per agreement between user and supplier on a case-by-case basis.					
Soft Error Rate	SER	E11	H, P, D, G	3	1		JEDEC Un- accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3	Applicable to devices with memory sizes ≥1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications. This test and its accept criteria is performed per agreement between user and supplier on a case-by-case basis. Final test report shall include detailed test facility location and altitude data.					
Lead (Pb) Free	LF	<u>E12</u>	Ŀ	<u>See Test</u> <u>Method</u>	<u>See Test</u> <u>Method</u>	<u>See Test</u> <u>Method</u>	AEC Q005	Applicable to ALL Pb-free devices. Note the recommendations for all related solderability, solder heat resistance and whisker requirements.					

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TEST GROUP F – DEFECT SCREENING TESTS														
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS						
Process Average Testing	ΡΑΤ	F1					AEC Q001	The supplier determines the sample sizes and accept criteria per the test methods. If these tests are not possible for a given part, the supplier must provide justification. The supplier determines the						
Statistical Bin/Yield Analysis	SBA	F2					AEC Q002	sample sizes and accept criteria per the test methods. If these tests are not possible for a given part, the supplier must provide justification. The supplier must perform some variant of PAT and SBA that meets the intent of the guideline.						
		TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS												
am 13 <sup>§TRESS</sup> 6567	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS						
Mechanical Shock	MS	G1	H, D, G	<u>15</u>	<u>1</u>	0 Fails	JEDEC JESD22-B104	Y1 plane only, 5 pulses, 0.5 msec duration, 1500 g peak acceleration. <b>TEST before and after at room temperature.</b>						
Variable Frequency Vibration	VFV	G2	H, D, G	<u>15</u>	<u>1</u>	0 Fails	JEDEC JESD22-B103	20 Hz to 2 KHz to 20 Hz (logarithmic variation) in >4 minutes, 4X in each orientation, 50 g peak acceleration. <b>TEST before and after at room temperature.</b>						
Constant Acceleration	СА	G3	H, D, G	<u>15</u>	<u>1</u>	0 Fails	MIL-STD-883 Method 2001	Y1 plane only, 30 K g-force for <40 pin packages, 20 K g-force for 40 pins and greater. <b>TEST before</b> and after at room temperature.						
Gross/Fine Leak	GFL	G4	H, D, G	<u>15</u>	<u>1</u>	0 Fails	MIL-STD-883 Method 1014	Any single-specified fine test followed by any single- specified gross test. For ceramic packaged cavity devices only.						
Package Drop	DROP	G5	H, D, G	5	1	0 Fails		Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface. This test is for MEMS cavity devices only. <b>TEST before and after</b> <b>DROP at room temperature.</b>						
Lid Torque	LT	G6	H, D, G	5	1	0 Fails	MIL-STD-883 Method 2024	For ceramic packaged cavity devices only.						
Die Shear	DS         G7         H, D, G         5         1         0 Fails         MIL-STD Method 2		MIL-STD-883 Method 2019	To be performed before cap/seal for all cavity devices.										
Internal Water Vapor		G8	H, D, G	<u>5</u>	1	0 Fails	MIL-STD-883 Method 1018	For ceramic packaged cavity devices only.						

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## Legend for Table 2

- Notes: **H** Required for hermetic packaged devices only.
  - **P** Required for plastic packaged devices only.
  - **B** Required Solder Ball Surface Mount Packaged (BGA) devices only.
  - N Nondestructive test, devices can be used to populate other tests or they can be used for production.
  - **D** Destructive test, devices are not to be reused for qualification or production.
  - S Required for surface mount plastic packaged devices only.
  - **G** Generic data allowed. See <u>Section 2.3 and Appendix 1.</u>
  - K Use method AEC-Q100-005 for preconditioning a stand-alone Non-Volatile Memory integrated circuit or an integrated circuit with a Non-Volatile Memory module.
  - <u>L</u> <u>Required for Pb-free devices only.</u>
  - **#** Reference Number for the particular test.
  - \* All electrical testing before and after the qualification stresses are performed to the limits of the individual device specification in temperature and limit value.

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## Table 3: Process Change Qualification Guidelines for the Selection of Tests **Physical Dimensions**

- A2 Temperature Humidity Bias or HAST
- A3 Autoclave or Unbiased HAST
- Temperature Cycling A4
- A5 Power Temperature Cycling
- A6 High Temperature Storage Life
- B1 High Temperature Operating Life
- Early Life Failure Rate B2
- B3 NVM Endurance, Data Retention
- C1 Wire Bond Shear
- C2 Wire Bond Pull
- C3 Solderability

- Solder Ball Shear C5
- Lead Integrity C6

C4

- Electromigration D1
- Time Dependent Dielectric Breakdown D2
  - D3 Hot Carrier Injection
  - Negative Bias Temperature Instability D4
- Stress Migration D5
- Human Body Model ESD E2
- Charged Device Model ESD F3
- E4 Latch-up

- **Electrical Distribution** E5
- Characterization E7
- Electromagnetic Compatibility E9
- E10 Short Circuit Characterization
- Soft Error Rate E11
- E12 Lead Free
- G1-4 Mechanical Series
- Package Drop G5
- G6 Lid Torque
- Die Shear G7
- G8 Internal Water Vapor

Note: A letter or "•" indicates that performance of that stress test should be considered for the appropriate process change. Reason for not performing a considered test should be given in the qualification plan or results.

																																	_
Table 2 Test #	A2	A3	A4	A5	A6	B1	B2	B3	G	C2	C3	C4	C5	C6	<b>D</b> 1	D2	D3	D4	D5	E2	E3	E4	E5	E7	E9	E10	E11	E12	5 <del>2</del>	G5	G6	G7	89 89
Test Abbreviation	THB	AC	тс	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	PD	SBS		EM	TDDB	нсі	NBTI	SM	HBM	CDM	LU	ED	CHAR	EMC	sc	SER	<u>LF</u>	MECH	DROP	Ц	DS	IWV
DESIGN																																	
Active Element Design		٠	•	М		•	•	DJ							D	D	D	D	D	٠	٠	•	•	•	٠	•	•			F			
Circuit Rerouting			Α	М																•	٠	٠	٠	•	•	•							
Wafer Dimension / Thickness			Е	М		•	•		Е	Е								٠		Е	Е	Е	•										
WAFER FAB																																	
Lithography	•		•	М		•	G		•	٠								٠				4	•										
Die Shrink	٠	•		М		٠	•	DJ							•	٠	٠	٠	٠	٠	٠	•	•	•	٠	٠	•						
Diffusion/Doping				М		•	G											٠		•	•	•	•	•									
Polysilicon			•	М		•		DJ										٠		•	•	•	•	•									
Metallization / Vias / Contacts	•	٠	•	М		•			٠	٠					٠				•		2	V	٠	٠		٠							
Passivation / Oxide / Interlevel Dielectric	к	к	•	М		•	GN	DJ	к	•						•	•	•	•	•	•	•	•	•									
Backside Operation			•	М		٠											X			M	М	٠		•					Н			Н	
FAB Site Transfer	٠	•	•	М		٠	•	J	٠	٠					•	•	•	•	•	٠	٠	٠	٠						Н			Н	
ASSEMBLY																																	
Die Overcoat / Underfill	•	•	•	М	•	•									2												•						Н
Leadframe Plating	•	٠	•	М	•					С	٠			•														F				Н	
Bump Material / Metal System	•	٠	•	М	•	•						•	•	K													•	F					
Leadframe Material		•	•	М	•					٠	•			•												٠		L	Н			Н	
Leadframe Dimension		٠	•	Μ							•	•	25	•												٠		F	Н				
Wire Bonding	•	٠	•	Q	•				٠	٠													М			•			Н				
Die Scribe/Separate	•	٠	•	Μ																													
Die Preparation / Clean	•	٠		Μ		•			•	•																						Н	
Package Marking											В																						
Die Attach	•	٠	•	Μ		•																	٠			٠		Ŀ	Н			Н	Н
Molding Compound	•	٠	•	Μ	٠	•	•				٠	٠		•													•	Ŀ					
Molding Process	٠	•	•	М	•	٠					٠	٠		•														F					
Hermetic Sealing		Н	Н		Н							Н		Н															Н		Н		Н
New Package	٠	•	•	М	•	•	•		•	٠	•	•	Т	•		l	l		l	٠	٠		•		l	•		L	Н	l	l	Н	Н
Substrate / Interposer	•	•	•	М	•	•	1	ĺ	•	•		l	Т			l	l		l	l	l				l	l		L	Н	l	l	Н	Н
Assembly Site Transfer	•	•	•	М	P	•	•		•	٠	•	٠	Т	٠									•					Ē	Н			Н	Н

- Only for peripheral routing Α
- For symbol rework, new cure time, temp В С If bond to leadfinger
  - G Н

F

- MEMS element only Only from non-100% burned-in parts
- Hermetic only
- EPROM or E<sup>2</sup>PROM
- J Κ Passivation only

- For Pb-free devices only Т
- For devices requiring PTC Μ
- Passivation and gate oxide Ν
- Q Wire diameter decrease
- Т For Solder Ball SMD only
- 联系方式:xuvj@bPage-18.0fo42 1391716567
- Е Thickness only

D

- Design rule change

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## Appendix 1: Definition of a <u>Product</u> Qualification Family

AECQ100 provides the following guideline for use of generic data to accelerate and streamline the gualification process for suppliers and customers. Suppliers and customers can use this guideline to reach mutual agreement on how to utilize generic data when it is appropriate.

For devices to be categorized in a product qualification family, they all must share the same major product, process and materials elements as defined below. The qualification of a particular product will be defined within, but not limited to, the categories listed below. Critical product functional details as defined in Section A1.1 and critical process steps and materials as defined in Sections A1.2 and A1.3 do not need to be matched exactly, but shall cover worst cases in application of the family generic data through technical justification.

All <u>products</u> in the same <u>product</u> qualification family are qualified by association when one family member successfully completes qualification with the exception of the device specific requirements of <u>Section 4.2</u>.

For broad changes that involve multiple attributes (e.g., site, materials, processes), refer to <u>Section A1.5</u> of this appendix and <u>Section 2.3</u> of Q100, which allows for the selection of worst-case test vehicles to cover all the possible permutations.

## A1.1 Product

- a. Product functionality (e.g., Op-Amp, regulator, microprocessor, Logic HC/TTL)
- b. Operating supply voltage range(s)
- c. Specified operating temperature range
- d. Specified operating frequency range
- e. Design library cells for the fab technology
  - <u>Memory IP (e.g., cell structure, building block)</u>
  - Digital design library cells (e.g., circuit blocks, IO modules, ESD cells) and/or analog design library cells (e.g., active circuit elements, passive circuit elements) at data sheet voltage level(s) and at data sheet or better temperature range, and power dissipation
  - Speed/performance of the library cells
- f. Memory type(s) and sizes
- g. Design rules for active circuits under pads
- h. Other functional characteristics as defined by supplier

For parts specified to operate at different power supplies (e.g., 5.0 V and 3.3 V), product qualification family data should be presented for both supply ranges.

For parts specified to operate at different temperature range, three (3) lots of data from the product gualification family at the temperature of the device in the data sheet need to be presented with Table 2 E1 TEST data. Stress classification at the temperature specified Q100 Table 2 groups A, B, E, and G must be equal or higher than device qualified. Three (3) lots of data from the product family at the frequency of the device in the data sheet need to be presented with Table 2 E1 TEST data at the temperature specified Q100 Table 2 groups A, B, E, and G must be equal or higher than device qualified. Three (3) lots of data from the product family at the frequency of the device in the data sheet need to be presented with Table 2 E1 TEST data at the temperature specified Q100 Table 2 groups A, B, E, and G. All memory types must be demonstrated to be qualified over three (3) lots using largest memory size to be qualified for devices in the family. If the part to be qualified has a larger memory size than the one already qualified, the supplier must perform at least one lot of testing on the larger memory configuration.

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## A1.2 Fab Process

Each process technology (e.g., CMOS, NMOS, Bipolar) must be considered and qualified separately. No matter how similar, processes from one fundamental fab technology cannot be used for another. For BiCMOS devices, data must be taken from the appropriate technology based on the circuit under consideration.

<u>"Worst case"</u> <u>family</u> requalification with the appropriate tests is required when the process or a material is changed (see Table A1 for guidelines). The important attributes defining a <u>fab process</u> are listed below:

- a. Wafer Fab Technology (e.g., CMOS, NMOS, Bipolar)
- b. Wafer Fab Process consisting of the same attributes listed below:
  - Circuit element feature size (e.g., layout design rules, die shrinks, contacts, gates, isolations)
  - Substrate (e.g., orientation, doping, epi, wafer size)
  - Number of masks (supplier must show justification for waiving this requirement)
  - Lithographic process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)
  - Doping process (e.g., diffusion vs. ion implantation)
  - Gate structure, material and process (e.g., polysilicon, metal, salicide, wet vs. dry etch)
  - Polysilicon material, thickness range & number of levels
  - Oxidation process and thickness range (e.g., gate & field oxides)
  - Interlayer dielectric material & thickness range
  - Metallization material, thickness range & number of levels
  - Passivation process (e.g., passivation oxide opening), material, & thickness range
  - Die backside preparation process <u>&</u> metallization

#### c. Wafer Fab Site

#### A1.3 Assembly Process - Plastic or Ceramic

The processes for plastic and ceramic package technologies must be considered and qualified separately. For devices to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification with the appropriate tests is required when the process or a material is changed. The supplier must submit technical justification to the user to support the acceptance of generic data with pin (ball) counts, die sizes, substrate dimensions/material/thickness, paddle sizes and die aspect ratios different than the device to be qualified. The supplier must possess technical data to justify the acceptance of generic data. The important attributes defining a qualification family are listed below:

- a. Package Type (e.g., DIP, SOIC, PLCC, QFP, PGA, PBGA)
  - Worst case within same package type (e.g., package warpage due to coefficients of thermal expansion mismatch)
  - Range of paddle (flag) size (maximum <u>&</u> minimum dimensions) qualified for the die size/aspect ratio under consideration
  - Substrate base material (e.g., PBGA)
- b. Assembly Process consisting of the same attributes listed below:
  - Leadframe base material
  - Leadframe plating process & material (internal & external to the package)
  - Die header / Thermal pad material
  - Die attach material
  - Wire bond material <u>& diameter</u>
  - <u>Wire bond method</u>, presence of downbonds, <u>&</u> process

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- Plastic mold compound <u>material</u>, organic substrate material, or ceramic package material
- Solder Ball metallization system (if applicable)
- Heatsink type, material, <u>& dimensions</u>
- Plastic Mold Compound Supplier/ID
- Die Preparation/Singulation
- c. Assembly Site

## A1.4 Qualification/Regualification Lot Reguirements

## Table A1.1: Part Qualification/Requalification Lot Requirements

Part Information	Lot Requirements for Qualification
New device and no applicable generic data.	Lot and sample size requirements per Table 2.
A part in a <u>product</u> family is qualified <u>with 3 lots</u> of <u>generic data</u> . The part to be qualified is less complex and meets the <u>product</u> Family Qualification Definition per Appendix 1.	Only device specific tests as defined in <u>Section</u> 4.2 are required. Lot and sample size requirements per Table 2 for the required tests.
<u>A part in a product family is qualified with 3 lots</u> of generic data. The part to be qualified is slightly more complex, with similar product functionality, meeting the product family qualification definition per Appendix 1. Examples for one (1) lot wafer / assembly qualification, would be, increasing ADC performance from 12 to 14 bits or package pin count from 16 to 20.	Review Table 3 to determine which tests from Table 2 should be considered. One (1) lot wafer / assembly lot and sample sizes per Table 2 for the required tests.
Part process change.	Review Table 3 to determine which tests from Table 2 should be considered. Lot and sample sizes per Table 2 for the required tests.
Part was environmentally tested to all the test extremes, but was electrically end-point tested at a temperature less than the Grade required.	The electrical end-point testing on at least <u>3 lots</u> (that completed qualification testing) must meet or exceed the temperature extremes for the device Grade required. Sample sizes shall be per Table 2.
Qualification/Requalification involving multiple sites.	Refer to Appendix 1, Section A1.5.
Qualification/Requalification involving multiple families.	Refer to Appendix 1, Section A1.5.

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## Table A1.2: Examples for Generic Data Use

The cases listed in the generic data portion of the table signify those scenarios in which a product and site combination has been previously qualified and generic data exists. The use options of generic data described in each case define the allowable generic data for device A<sub>n</sub> in the qualification portion of the table.

Guidelines for using Table A1.2:

- 1. Product An is a product to be qualified that belongs to Product Family A.
- Product A<sub>1</sub> should be representative of the product family, possibly a more complex case family part (e.g., 60V regulator vs. 45V regulator, 8 channel vs. 4 channel amplifier) that would cover most, if not all, other family parts.
- 3. <u>Same Fab is same process node and materials</u>. <u>Different Fab has one or more different process</u> <u>elements</u>.
- 4. <u>Same Assembly is same process, materials and package type</u>. <u>Different Assembly has one or more different process, material elements or package elements</u>.
- 5. New test is qualification tests per Section 4.1
- 6. Fab process C<sub>1</sub> is the same as C except for one or more different elements (e.g., Al to Cu metal).
- 7. <u>Assembly process E<sub>1</sub> is the same as E except for one or more different elements (e.g. Al to Cu bond wire, mold compound).</u>
- 8. Product B is functionally different from Product A (e.g., logic vs. analog, voltage regulator vs. amplifier).
- 9. Increased product complexity can decrease the applicability for portion of the table below.

## New Qualification Scenario (Definition of Part to be Qualified)

<u>Case</u>	<b>Description</b>	<u>Product</u>	Fab Site	<u>Assembly</u> <u>Site</u>	<u>Min. Lots of</u> Data Needed for Qualification	Product/Process (defined in Appendix A1)
<u>New</u> <u>Device /</u> <u>Product</u>	This is the unqualified device / product	<u>A</u> n	<u>C</u>	E	3	<ul> <li><u>1 lot ESD and LU; 3 lots</u> <u>ED AC(E) and 1 lot HTOL</u> <u>minimum on A<sub>n</sub>CE in</u> <u>addition to below for all</u> <u>cases</u></li> </ul>

## Previously Qualified Scenario (Existing Generic Data)

<u>Case</u>	Description	Product	Fab Site	Assembly Site	Lots of Generic Data Available	Use Options of Generic Data
<u>1</u>	<u>B from a different</u> product family	B	<u>c</u>	Ē	<u>3</u>	<u>No Option</u> ● <u>3 lots A<sub>n</sub>CE (new test)</u>
<u>2A</u>	B from a different		<u>C</u>	<u>F</u>	<u>3</u>	<ul> <li><u>No Option</u></li> <li><u>3 lots using A<sub>n</sub> (new test)</u></li> </ul>
<u>2B</u>	product family	B	D	Ē	<u>3</u>	No Option • <u>3 lots A<sub>n</sub>CE (new test)</u>
<u>3</u>	Different Fab Process and different site as A <sub>1</sub> Different Assembly and different site as A <sub>1</sub>	<u>A</u> 1	D	Ē	<u>3</u>	No Option • <u>3 lots using A<sub>n</sub> (new test)</u>

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## Table A1.2: Examples for Generic Data Use (Continued)

<u>Case</u>	Description	Product	Fab Site	<u>Assembly</u> <u>Site</u>	Lots of Generic Data Available	Use Options of Generic Data
<u>4A</u>	One or more elements of the fab process is different than the base process Same Assembly Process and site as A <sub>1</sub>		<u>C</u> 1	Ē	<u>3</u>	<ul> <li><u>3 lots A<sub>n</sub>CE (new test)</u> <u>OR</u></li> <li><u>2 lots A<sub>n</sub>CE (new test)</u> <u>+ 2 lots A<sub>1</sub>C<sub>1</sub>E (generic)</u> <u>OR</u></li> <li><u>1 lot A<sub>n</sub>CE (new test)</u> <u>+ 3 lots A<sub>1</sub>C<sub>1</sub>E (generic)</u></li> </ul>
<u>4B</u>	Same Fab Process and same site as A <sub>1</sub> One or more elements of the assembly process is different than the base process E	<u>A</u> 1	<u>C</u>	<u>E</u> 1	<u>3</u>	• $\frac{3 \text{ lots } A_n \text{CE} (\text{new test})}{\text{OR}}$ • $\frac{2 \text{ lots } A_1 \text{CE} (\text{new test})}{+ 2 \text{ lots } A_1 \text{CE}_1 (\text{generic})}$ • $\frac{1 \text{ lot } A_1 \text{CE} (\text{new test})}{+ 3 \text{ lots } A_1 \text{CE}_1 (\text{generic})}$
<u>5A</u>	Same Fab Process and site as An Same Assembly Process but different site as An	•	<u>C</u>	Ē	3	<ul> <li><u>3 lots A<sub>n</sub>CE (new test)</u> <u>OR</u></li> <li><u>2 lots A<sub>n</sub>CE (new test)</u> + 2 lots A<sub>1</sub>CF (generic) <u>OR</u></li> <li><u>1 lot A<sub>n</sub>CE (new test)</u> + 3 lots A<sub>1</sub>CF (generic)</li> </ul>
<u>5B</u>	Same Fab Process, but different site as A <sub>n</sub> Same Assembly Process and site as A <sub>n</sub>	<u>A</u> 1	D		<u>3</u>	<ul> <li><u>3 lots A<sub>n</sub>CE (new test)</u> <u>OR</u></li> <li><u>2 lots A<sub>n</sub>CE (new test)</u> + 2 lots A<sub>1</sub>DE (generic) <u>OR</u></li> <li><u>1 lot A<sub>n</sub>CE (new test)</u> + 3 lots A<sub>1</sub>DE (generic)</li> </ul>
<u>6</u>	Same Fab Process and site as A <sub>n</sub> Same Assembly Process and site as A <sub>n</sub>	<u>A</u> 1	<u>C</u>	Ē	<u>3</u>	<ul> <li><u>3 lots A<sub>1</sub>CE (Generic)</u></li> </ul>

## Previously Qualified Scenario (Existing Generic Data) (continued)

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## A1.5 Qualification of <u>Changes in</u> Multiple Sites and Families

#### A1.5.1 Multiple Sites

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

#### A1.5.2 Multiple Families

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab family or assembly family, the qualification test vehicles should be: 1) One lot of a single device type from each of the families that are projected to be most sensitive to the changed attribute, or 2) Three lots total (from any combination of acceptable generic data and stress test data) from the most sensitive families if only one or two families exist.

Below is the recommended process for qualifying changes across many process and product families:

- a. Identify all products affected by the proposed process changes.
- b. Identify the critical structures and interfaces potentially affected by the proposed process change.
- c. Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces (see the example in Table A1<u>.3</u>). Note that steps (a) to (c) are equivalent to the creation of an FMEA.
- d. Define the product groupings or families based upon similar characteristics as they relate to the structures and device sensitivities to be evaluated, and provide technical justification to document the rationale for these groupings.
- e. Provide the qualification test plan, including a description of the change, the matrix of tests, and the representative products, that will address each of the potential failure mechanisms and associated failure modes.
- f. Robust process capability must be demonstrated at each site (e.g., control of each process step, capability of each piece of equipment involved in the process, equivalence of the process stepby-step across all affected sites) for each of the affected process steps.

## Table A1.3: Example of Failure Mode/Mechanism List for a Passivation Change

Critical Structure or Interface	Potential Failure Mechanism	Associated Failure Modes	On These Products
Passivation to Mold	Passivation Cracking - Corrosion	Functional Failures	All Die
Compound Interface	Mechanism         N           old         Passivation Cracking - Corrosion         Function           Mold Compound - Passivation Delamination         Corner Fassivation Delamination         Function           Stress-Induced Voiding         Function         Function           ace         Ionic Contamination         Leakage	Corner Wire Bond Failures	Large Die
Passivation to	Stress-Induced Voiding	Functional Failures	Die with Minimum Width Metal Lines
Metallization Interface	Potential Failure MechanismAssociated Failu ModesPassivation Cracking - CorrosionFunctional FailureMold Compound - Passivation DelaminationCorner Wire Bong FailuresStress-Induced VoidingFunctional FailureIonic ContaminationLeakage, Paramet ShiftsPiezoelectric LeakageParametric Shifts (e Resistance, Gain, Or	Leakage, Parametric Shifts	All Die
Polysilicon and Active Resistors	Piezoelectric Leakage	Parametric Shifts (e.g., Resistance, Gain, Offset)	Analog Products

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## Appendix 2: Q100 Certification of Design, Construction and Qualification

#### Supplier Name:

Date:

The following information is required to identify a device that has met the requirements of AEC-Q100. Submission of the required data in the format shown below is optional. All entries must be completed; if a particular item does not apply, enter "Not Applicable". This template can be downloaded from the AEC website at http://www.aecouncil.com.

#### This template is available as a stand-alone document.

	Item Name	Supplier Response
1.	User's Part Number:	
2.	Supplier's Part Number/Data Sheet:	
3.	Device Description:	
4.	Wafer/Die Fab Location & Process ID: a. Facility name/plant #:	
	b. Street address:	
	c. Country:	
5.	Wafer Probe Location:	
	a. Facility name/plant #:	
	b. Street address:	
6	C. Country. Assembly Location & Process ID:	
0.	a Facility name/plant #	
	b. Street address:	
	c. Country:	
7.	Final Quality Control A (Test) Location:	AKKL .
	<ul> <li>a. Facility name/plant #:</li> </ul>	
	b. Street address:	X
	c. Country:	
8.	Wafer/Die:	XZ
	a. Water size:	XXT
	D. Die lanniy. c. Die mask set revision & name:	<b>ム-X</b>
	d Die photo:	See attached
9.	Wafer/Die Technology Description:	
	a. Wafer/Die process technology:	
	b. Die channel length:	
	c. Die gate length:	$\sim$
	d. Die supplier process ID (Mask #):	
	e. Number of transistors or gates:	
10	t. Number of mask steps:	
10.	a Die width:	
	b Die length:	
	c. Die thickness (finished):	
11.	Die Metallization:	
	a. Die metallization material(s):	
	b. Number of layers:	
	c. Thickness (per layer):	
	d. % of alloys (if present):	

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12. Die Passivation:	
a. Number of passivation layers:	
b. Die passivation material(s):	20 C
c. Thickness(es) & tolerances:	
13. Die Overcoat Material (e.g., Polyimide):	
14. Die Cross-Section Photo/Drawing:	See attached Not available
15. Die Prep Backside:	
a. Die prep method:	
b. Die metallization:	
c. Thickness(es) & tolerances:	
16. Die Separation Method:	
a. Kerf width (μm):	
<li>b. Kerf depth (if not 100% saw):</li>	
c. Saw method:	Single 📋 Dual 📋
17. Die Attach:	
a. Die attach material ID:	
b. Die attach method:	
c. Die placement diagram:	See attached Not available
18. Package:	
a. Type of package (e.g., plastic, ceramic,	
unpackaged):	
D. Ball/lead court:	
(-1.000)	115
u. Leau (Fb) nee (< 0.1 % nonogenous material):	
e Package outline drawing:	
19 Mold Compound:	
a. Mold compound supplier & ID:	X
b. Mold compound type:	
c. Flammability rating:	UL 94 V1 🖸 🔨 UL 94 V0 🔲
d. Fire Retardant type/composition:	
e. Tg (glass transition temperature)(°C):	
f. CTE (above & below Tg)(ppm/°C):	CTE1 (above Tg) = CTE2 (below Tg) =
20. Wire Bond:	
a. Wire bond material:	
b. Wire bond diameter (mils):	
c. Type of wire bond at die:	
d. Type of wire bond at leadframe:	
e. Wire bonding diagram:	See attached Not available
21. Leadframe (if applicable):	
a. Paddle/flag material:	
b. Paddle/flag width (mils):	
c. Paddle/flag length (mils):	
a. Paddle/flag plating composition:	
e. Paddle/flag plating thickness (μinch):	
Leadframe handing plating compacition:	
<ul> <li>g. Leauname bonding plating composition:</li> <li>b. Loadframe bonding plating thickness.</li> </ul>	
(uinch):	
i External lead plating composition:	
i External lead plating thickness (uinch):	
j. $\Box_{\lambda}$ is a planet	

22. Substrate (if applicable):	
a. Substrate material (e.g., FR5, BT):	
b. Substrate thickness (mm):	
c. Number of substrate metal layers:	2 million and a second s
d. Plating composition of ball solderable	
A Panel singulation method:	
f Solder ball composition	
g. Solder ball diameter (mils):	
23. Unpackaged Die (if not packaged):	
a. Under Bump Metallurgy (UBM)	
composition:	
b. Thickness of UBM metal:	
c. Bump composition:	
d. Bump size:	
24. Header Material (if applicable):	
25. Thermal Resistance:	
a. $\theta_{JA} \circ C/W$ (approx):	
b. θ <sub>JC</sub> °C/W (approx):	
c. Special thermal dissipation construction	
Techniques:	
26. Test circuits, bias levels, & operational conditions imposed during the supplier's life	Son attached
and environmental tests:	
27 Fault Grade Coverage (%)	% Not digital circuitry
28 Maximum Process Exposure Conditions:	* Note: Temperatures are as measured on the center of
	the plastic package body top surface.
a. MSL @ rated SnPb temperature:	at °C (SnPb)
b. MSL @ rated Pb-free temperature:	at °C (Pb-free)
c. Maximum dwell time @ maximum	
process temperature:	
Attachments:	Requirements:
Die Photo	1 According Contification of Design Construction
Backago Outlino Drawing	A separate Certification of Design, Construction     Solution P(N)
	wafer fab, and assembly location
Die Cross-Section Photo/Drawing	water tab, and assembly location.
Wire Bonding Diagram	2 Decian Construction & Qualification shall be
	signed by the responsible individual at the supplier
	who can verify the above information is accurate
Lest Circuits, Blas Levels, &	and complete. Type name and sign below.
Conditions	-
Completed by: Date:	Certified by: Date:
Typed or	
Printed:	
Signature:	
///2	
Title:	
	•

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## Appendix 3: Plastic Package Opening for Wire Bond Testing

## A3.1 Purpose

The purpose of this Appendix is to define a guideline for opening plastic packaged devices so that reliable wire pull or bond shear results will be obtained. This method is intended for use in opening plastic packaged devices to perform wire pull testing after temperature cycle testing or for bond shear testing.

## A3.2 Materials and Equipment

#### A3.2.1 Etchants

Various chemical strippers and acids may be used to open the package dependent on your experience with these materials in removing plastic molding compounds. Red Fuming Nitric Acid has demonstrated that it can perform this function very well on novolac type epoxies, but other materials may be utilized if they have shown a low probability for damaging the bond pad material.

#### A3.2.2 Plasma Strippers

Various suitable plasma stripping equipment can be utilized to remove the plastic package material.

#### A3.3 Procedure

- a. Using a suitable end mill type tool or dental drill, create a small impression just a little larger than the chip in the top of the plastic package. The depth of the impression should be as deep as practical without damaging the loop in the bond wires.
- b. Using a suitable chemical etchant or plasma etcher, remove the plastic material from the surface of the die, exposing the die bond pad, the loop in the bond wire, and at least 75% of the bond wire length. Do not expose the wire bond at the lead frame (these bonds are frequently made to a silver plated area and many chemical etchants will quickly degrade this bond making wire pull testing impossible).
- c. Using suitable magnification, inspect the bond pad areas on the chip to determine if the package removal process has significantly attacked the bond pad metallization. If a bond pad shows areas of missing metallization, the pad has been degraded and shall not be used for bond shear or wire pull testing. Bond pads that do not show attack can be used for wire bond testing.

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## Appendix 4: Minimum Requirements for Qualification Plans and Results

The following information is required as a minimum to identify a device that has met the requirements of AEC-Q100 (see Appendix Templates 4A and 4B). Submission of data in this format is optional. However, if these templates are not used, the supplier must ensure that each item on the template is adequately addressed. The templates can be downloaded from the AEC website at http://www.aecouncil.com.

## A4.1 Plans

- 1. Part Identification: Customer P/N and supplier P/N.
- 2. Site or sites at which life testing will be conducted.
- 3. List of tests to be performed (e.g., JEDEC method, Q100 method, MIL-STD method) along with conditions. Include specific temperature(s), humidity, and bias to be used.
- 4. Sample size and number of lots required.
- 5. Time intervals for end-points (e.g., 0 hour, 500 hour, 1000 hour).
- 6. Targeted start and finish dates for all tests and end-points.
- 7. Supplier name and contact.
- 8. Submission date.
- 9. Material and functional details and test results of devices to be used as generic data for qualification. Include rationale for use of generic data.

## A4.2 Results

All of above plus:

- 1. Date codes and lot codes of parts tested.
- 2. Process identification.
- 3. Fab and assembly locations.
- 4. Mask number or designation.
- 5. Number of failures and number of devices tested for each test.
- 6. Failure analyses for all failures and corrective action reports to be submitted with results.

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# Appendix Template 4A: AEC-Q100 Qualification Test Plan

			QUALIFICATION	TESTFLAN				
USER COMPANY:				DATE:				
USER P/N:			TRACKING NUMBER:					
USER SPEC #:			R COMPONENT ENGINEER:					
SUPPLIER COMPANY:			R MANUFACTURING SITES:					
SUPPLIER P/N:			PPAP SUBMISSION DATE:					
SUPPLIER FAMILY TYPE:			RE	ASON FOR QUALIFICATION:				
STRESS TEST	ABV	TEST#	TEST METHOD	Test Conditions/S.S. per Lot/# Lots (identify temp, RH, & bias)	REQUIF S.S	REMENTS # LOTS	RESULTS Fails/S.S./# lots	
Preconditioning	PC	A1	JEDEC J-STD-020	Peak Reflow Temp. = Preconditioning used =	Min. N	/ISL = 3	MSL =	
Temperature Humidity Bias or HAST	THB / HAST	A2	JESD22-A101/A110		77	3		
Autoclave or Unbiased HAST	AC / UHST	A3	JESD22-A102/A118		77	3		
Temperature Cycle	тс	A4	JESD22-A104		77	3		
Power Temperature Cycling	PTC	A5	JESD22-A105		45	1		
High Temperature Storage Life	HTSL	A6	JESD22-A103		45	1		
High Temperature Operating Life	HTOL	B1	JESD22-A108		77	3		
Early Life Failure Rate	ELFR	B2	AEC Q100-008		800	3		
NVM Endurance, Data Retention, & Operational Life	EDR	B3	AEC Q100-005		77	3		
Wire Bond Shear	WBS	C1	AEC Q100-001		5	1		
Wire Bond Pull Strength	WBP	C2	MIL-STD-883 - 2011		5	1		
Solderability	SD	C3	JESD22-B102 J-STD-002D	8 hr steam aging prior to testing	15	1		
Physical Dimensions	PD	C4	JESD22-B100/B108		10	3		
Solder Ball Shear	SBS	C5	AEC Q100-010		10	3		
Lead Integrity	LI	C6	JESD22-B105	.50	5	1		
Electromigration	EM	D1						
Time Dependent Dielectric Breakdown	TDDB	D2						
Hot Carrier Injection	HCI	D3						
Negative Bias Temperature Instability	NBTI	D4						
Stress Migration	SM	D5	1					
Pre- and Post-Stress Electrical Test	TEST	E1	Test to spec					
ESD - Human Body Model	HBM	E2	AEC Q100-002		See Tes	st Method		
ESD - Charged Device Model	CDM	E3	AEC Q100-011		See Tes	st Method		
Latch-Up	LU	E4	AEC Q100-004		6	1		
Electrical Distributions	ED	E5	AEC Q100-009		30	3		
Fault Grading	FG	E6	AEC-Q100-007					
Characterization	CHAR	E7	AEC Q003					
Electromagnetic Compatibility	EMC	E9	SAE J1752/3		1	1		
Short Circuit Characterization	SC	E10	AEC Q100-012		10	3		
Soft Error Rate	SER	E11	JESD89-1, -2, -3		3	1		
Lead Free	<u>LF</u>	<u>E12</u>	<u>Q005</u>		<u> </u>			
Process Average Test	PAT	F1	AEC Q001		ļ			
Statistical Bin/Yield Analysis	SBA	F2	AEC Q002		ļ	-		
Hermetic Package Tests	MECH	G1-4	Series		15	1		
Package Drop –	DROP	G5			5	1		
Lid Torque	LT	G6	MIL-STD-883 - 2024		5	1		
Die Shear Strength	DS	G7	MIL-STD-883 - 2019		5	1		
Internal Water Vapor	IWV	G8	MIL-STD-883 - 1018		5	1		
Supplier:				Approved by: (User Engineer)				

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## Appendix Template 4B: AEC-Q100 Generic Data

bjective:			Package:		-			(	Qual Plan Ref #			
Device:			Fab/Assy/Test:		10	2			Date Prepared			
Cust PN: _ Maskset:			Device Engr: Product Engr:	-	-				Prepared by Date Approved			
Die Size:			Component Engr:						Approved by			
			End-Doint	Sample	# of	Total #	Part to bo	Difforoncos	Generic	Difforences	Gonorio	Differences
Test #	ABV	Q100 Test Conditions	Requirements	Size/Lot	# of Lots	Units	Qualified	from Q100	Family part A	from Q100	Family part B	from Q100
A1	PC	JEDEC J-STD-020	TEST = ROOM	All surface to A2	e mount 2, A3, A4	parts prior , A5						
A2	THB / HAST	JESD22-A101/A110	TEST = ROOM and HOT	77	3	231						
A3	AC / UHST	JESD22-A102/A118	TEST = ROOM	77	3	231						
A4	тс	JESD22-A104	TEST = HOT	77	3	231						
A5	PTC	JESD22-A105	TEST = ROOM and	45	1							
<b>A</b> 6	HTSL	JESD22-A103	TEST = ROOM and HOT	45	1							
B1	HTOL	JESD22-A108	TEST = ROOM, COLD <u>, and HOT</u>	77	3	231						
B2	ELFR	AEC Q100-008	TEST = ROOM and HOT	800	3	2400						
В3	EDR	AEC Q100-005	TEST = ROOM and HOT	77	3	231						
C1	WBS	AEC Q100-001	Cpk>1.5 and in SPC	An appro for each b	priate tir onder to	ne period be used						
C2	WBP	MIL-STD-883 – 2011								$\wedge$		
C3	SD	JESD22-B102 J-STD-002D	>95% solder coverage	15	1	15				$\langle \rangle$		
C4	PD	JESD22-B100/B108	Cpk > 1.5 per JESD95	10	3	30						
C5	SBS	AEC Q100-010	Two 220°C reflow cycles before SBS						V'Z	-		
C6	LI	JESD22-B105	No lead breakage or finish cracks	10 leads from each of 5	1	5			4			
D1	EM							$X/\lambda$				
D2	TDDB							K/				
D3	нсі											
D0	NDTI											
D4	NBII						$\sim$					
D5	SM											
E1	TEST		All parametric and functional tests	All units	-	All	N					
E2	НВМ	AEC Q100-002	TEST = ROOM and HOT		1	Var.						
E3	CDM	AEC Q100-011	TEST = ROOM and HOT	X	1	Var.						
E4	LU	AEC Q100-004	TEST = ROOM and HOT	6	1	6						
E5	ED	AEC Q100-009	TEST = ROOM, HOT, and COLD	30	3	90						
E6	FG	AEC Q100-007	X-X									
E7	CHAR	AEC Q003				-	1					
E9	EMC	SAE J1752/3		1	1	1						
E10	SC	AEC Q100-012		10	3	30						
E11	SER	JESD89-1, -2, -3		3	1	3						
E12	LF	<u>Q005</u>										
<b>F1</b>	PAT	AEC Q001		All units	-	All						
F2	SBA	AEC Q002		All units	-	All						
G1	MS	JESD22-B104	TEST = ROOM	<u>15</u>	1	<u>15</u>						
G2	VEV	JESD22-B103	TEST = ROOM	<u>15</u>	<u>1</u>	<u>15</u>						
G3	CA	MIL-STD-883 - 2001	TEST = ROOM	<u>15</u>	<u>1</u>	<u>15</u>						
G4	GFL	MIL-STD-883 – 1014		<u>15</u>	<u>1</u>	<u>15</u>						
G5	DROP		TEST = ROOM	5	1	5						
66		MIL-STD-883 - 2024		5	1	5						
60	105	MIL-51D-883 - 2019		5	1	5						
GÖ	1 V V	WIL-51D-883 - 1018		<u>5</u>		ব						

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## Appendix Template 4B: AEC-Q100 Generic Data (continued)

Part Attributes	Part to be Qualified	Generic Family <u>P</u> art A	Generic Family Part B								
User Part Number											
Supplier Part Number											
A1.1 Product											
Product Functionality (e.g., Op- Amp. Regulator, Microprocessor, Logic – HC/TTL)											
Operating Supply Voltage Range(s)											
Specified Operating Temperature Range	TOTON .										
Specified Operating Frequency Range											
<sup>1</sup> Analog <u>Design Library Cells (e.g.,</u> <u>active circuit elements, passive</u> circuit elements)											
<sup>1</sup> Digital <u>Design Library Cells (e.g.,</u> <u>circuit blocks, IO modules, ESD</u> cells)											
Memory IP (e.g., cell structure, building block)											
Memory Type(s) & Size(s)											
Design Rules for Active Circuits under Pads											
Other <u>Functional</u> Characteristics (as defined by supplier)											
	<u>A1.2 Fab</u>	Process	7								
Wafer Fab Technology (e.g., CMOS NMOS Bipolar)											
Circuit Element Feature Size (e.g.,		.60									
layout design rules, die shrinks, contacts, gates, isolations)		XAX									
Substrate (e.g., orientation, doping, epi, wafer size)		XX									
Maximum Number of Masks (supplier must show justification for waiving this requirement)		XX									
Lithographic Process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)	Λ	X.									
Doping Process (e.g., diffusion vs.											
Gate Structure, Material & Process (e.g., polysilicon, metal, salicide,	Ŵ										
Polysilicon Material, Thickness Pange & Number of Levels											
Oxidation Process & Thickness	-16-2										
Interlevel Dielectric Material &											
Metallization Material, Thickness											
Range, & Maximum Number of Levels											
Passivation Process (e.g.,											
Material, & Thickness Range											
Die Backside Preparation Process & Metallization											
Wafer Fabrication Site											

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## Appendix Template 4B: AEC-Q100 Generic Data (continued)

Part Attributes	Part to be Qualified	Generic Family Part A	Generic Family Part B							
A1.3 Assembly Process – Plastic or Ceramic										
Assembly Site										
Package Type <u>(e.g., DIP, SOIC,</u> <u>QFP, PGA, PBGA)</u>										
Range of Paddle/Flag Size (maximum & minimum dimensions) Qualified for the Die Size/Aspect Ratio Under Consideration	D									
Worst Case Package (e.g., package warpage due to CTE mismatch)										
Substrate Base Material (e.g., PBGA)										
Leadframe <u>Base Material</u>										
Die Header / Thermal Pad Material										
Lead <u>frame Plating Material &amp;</u> <u>Process (internal &amp; external to the</u> <u>package)</u>										
Die Attach Material										
Wire Bond Material & Diameter										
Wire Bond Method, Presence of Downbonds, & Process										
Plastic Mold Compound Material, Organic Substrate Material, or Ceramic Package Material										
Plastic Mold Compound Supplier/ID										
Solder Ball Metallization System (if applicable)										
Heatsink Type, Material, & Dimensions		X X								
Die Preparation/Singulation		\								

Note 1: Design Library cells need to follow guidelines for temperature ranges, voltage ranges, speed, performance, and power dissipation as defined in Appendix 1.

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## Appendix 5: Part Design Criteria to Determine Need for EMC Testing

- A5.1 Use the following criteria to determine if a part is a candidate for EMC testing:
  - a. Digital technology, LSI, products with oscillators or any technology that has the potential of producing radiated emissions capable of interfering with communication receiver devices. Examples include microprocessors, high speed digital IC's, FET's incorporating charge pumps, devices with watchdogs, and switch-mode regulator control and driver IC's.
  - b. All new, requalified, or existing IC's that have undergone revisions from previous versions that have the potential of producing radiated emissions capable of interfering with communication receiver devices.
- A5.2 Examples of factors that would be expected to affect radiated emissions:
  - Clock drive (internal or external) I/O Drive
  - Manufacturing process or material composition that reduces rise/fall times (e.g., lower E dielectric, lower p metallization)
  - Minimum feature size (e.g., die shrink)
  - Package or pinout configuration
  - Leadframe material

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## Appendix 6: Part Design Criteria to Determine Need for SER Testing

- A6.1 Use the following criteria to determine if a part is a candidate for SER Testing:
  - a. The part use application will have a significant radiation exposure such as an aviation application or extended service life at higher altitudes.
  - b. SER testing is needed for devices with large numbers of SRAM or DRAM cells (≥ 1 Mbit). For example: Since the SER rates for a 130 nm technology are typically near 1000 FIT/MBIT, a device with only 1,000 SRAM cells will result in an SER contribution of ~1 FIT.
- A6.2 Examples of factors that would be expected to affect SER results:
  - a. Technology shrink to small Leffective.
  - b. Package mold/encapsulate material.
  - c. Bump material making die to package connections for Flip Chip package applications.
  - d. Mitigating factors such as implementation of Error Correcting Code (ECC) and Soft Error Detection (SED).
- A6.3 Cases where new SER testing may be required:
  - a. Change in basic SRAM/DRAM transistor cell structure (e.g., L<sub>eff</sub>, well depth and dopant concentration, isolation method).

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## Appendix 7: AEC-Q100 AND THE USE OF MISSION PROFILES

## A7.1 SCOPE

Successful completion of the test requirements in Table 2 allows the claim to be made that the part is AEC Q100 qualified. Additional testing may be agreed between Component Manufacturers and Tier 1 Component Users depending on more demanding application environments. To address these more stringent conditions, application based Mission Profiles may be used for a reliability capability.

A mission profile is the collection of relevant environmental and functional loads that a component will be exposed to during its use lifetime.

## A7.1.1 Purpose

This appendix provides information on an approach that can be used to assess the suitability of a component for a given application and its mission profile for unique requirements. The benefit of applying this approach is that, in the end, the reliability margin between the component (specification) space and the application (condition) space may be shown.

- Section A7.2 demonstrates the relation between AEC-Q100 stress conditions / durations and a typical example of a set of use life time and loading conditions.
- Section A7.3 describes the approach, supported by flow charts, which can be used for a reliability capability assessment starting from a mission profile description.

## A7.1.2 References

- <u>SAE J1879/J1211/ZVEI Handbook for Robustness Validation of Semiconductor Devices</u> in Automotive Applications
- JEDEC JEP122 Failure Mechanisms and Models for Semiconductor Devices

## A7.2 BASE CONSIDERATIONSE

#### A7.2.1 Use Lifetime and Mission Profile

The use lifetime assumptions drawn here are an example used for demonstration purpose only. Many typical mission profiles will differ in one or more characteristics from what is shown below.

- <u>service lifetime in years</u>
- engine on-time in hours
- engine off time { idle} in hours
- <u>non-operating time in hours</u>
- <u>number of engine on-off cycles</u>
- service mileage

The mission profile itself is generated by adding information on thermal, electrical, mechanical and any other forms of loading under use conditions to the above lifetime characteristics. Examples of these and how they relate to the test conditions in Table 2 are shown in Table A7.1.

## A7.2.2 Relation to AEC-Q100 Stress Test Conditions and Durations

The basic calculations in Table A7.1 for each of the major stress tests demonstrate how one can derive suitable test conditions for lifetime characteristics based on reasonable assumptions for the loading. Caution should always be taken on use of excessive test conditions beyond those in Table 2, because they may induce unrealistic fail mechanisms and/ or acceleration.

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## A7.3 METHOD TO ASSESS A MISSION PROFILE

This section demonstrates how to perform a more detailed reliability capability assessment in cases where the application differs significantly from existing and proven situations:

- <u>Application has a demanding loading profile</u>
- Application has an extended service lifetime requirement
- Application has a more stringent failure rate target over lifetime

These considerations may result in extended test durations. In addition, there may be components manufactured in new technologies and/or containing new materials that are not yet gualified. In such cases, unknown failure mechanisms may occur with different times-to-failure which may require different test methods and/or conditions and/or durations.

For these cases, two flow charts are available to facilitate both Tier 1 and Component Manufacturing in a reliability capability assessment:

- Flow Chart 1 in Figure A7.1 describes the process at Component Manufacturer to assess whether a new component can be qualified by AEC-Q100.
- Flow Chart 2 in Figure A7.2 describes (1) the process at Tier 1 to assess whether a certain electronic component fulfills the requirements of the mission profile of a new Electronic Control Unit (ECU); and (2) the process at Component Manufacturer to assess whether an existing component qualified according to AEC-Q100 can be used in a new application.

For details on how to apply this method, please refer to SAE J1879, SAE J1211, and/or ZVEI Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications.

In summary, the flow charts result in the following three clear possible conclusions:

- [A] AEC-Q100 test conditions do apply.
- [B] Mission Profile specific test conditions may apply.
- [C] Robustness Validation may be applied with detailed alignment between Tier1 and Component Manufacturer.

In addition, not shown in the flow charts, the expected end of life failure rate may be an important criterion. Regarding failure rates, the following points should be considered:

- No fails in 231 devices (77 devices from 3 lots) are applied as pass criteria for the major environmental stress tests. This represents an LTPD (Lot Tolerance Percent Defective) = 1, meaning a maximum of 1% failures at 90% confidence level.
- This sample size is sufficient to identify intrinsic design, construction, and/or material issues affecting performance.
- <u>This sample size is NOT sufficient or intended for process control or PPM evaluation.</u> <u>Manufacturing variation failures (low ppm issues) are achieved through proper process</u> <u>controls and/or screens such as described in AEC-Q001 and AEC-Q002.</u>
- <u>Three lots are used as a minimal assurance of some process variation between lots.</u> A monitoring process has to be installed to keep process variations under control.
- Sample sizes are limited by part and test facility costs, qualification test duration and limitations in batch size per test.

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## Table A7.1: Basic Calculations for AEC-Q100 Stress Test Conditions and Durations

	Loading	Mission Profile Input	Stress Test	Stress Conditions	Acceleration Model (all temperatures in K, not in °C)	Model Parameters	Calculated Test Duration	Q100 Test Duration
	<u>Operation</u>	$\underline{t_u = 12,000 \text{ hr}}$ $\underline{(average operating use}$ $\underline{time over 15 \text{ yr}}$ $\underline{T_u = 87 ^{\circ}C}$ $\underline{(average junction}$ $\underline{temperature in use}$ $\underline{environment}$	<u>High</u> <u>Temperature</u> <u>Operating</u> <u>Life</u> (HTOL)	$\underline{T_t} = 125 \text{ °C}$ <u>(junction</u> <u>temperature in</u> <u>test</u> <u>environment)</u>	<u>Arrhenius</u> $A_{t} = \exp\left[\frac{E_{a}}{k_{B}} \cdot \left(\frac{1}{T_{u}} - \frac{1}{T_{t}}\right)\right]$ <u>Also applicable for High</u> <u>Temperature Storage Life (HTSL)</u> <u>and NVM Endurance, Data</u> <u>Retention Bake, &amp; Operational Life</u> (EDR)	$\frac{E_a = 0.7 \text{ eV}}{(\text{activation energy; } 0.7 \text{ eV is a}}$ $\frac{\text{typical value, actual values}}{\text{depend on failure mechanism and}}$ $\frac{\text{range from -0.2 to } 1.4 \text{ eV}}{\frac{K_B = 8.61733 \text{ x } 10^{-5} \text{ eV/K}}{(\text{Boltzmann's Constant})}}$	$\frac{t_{i} = 1393 \text{ hr}}{(\text{test time})}$ $t_{i} = \frac{t_{u}}{A_{f}}$	<u>1000 hr</u>
-sł	<u>Thermo-</u> mechanical	$\frac{n_{u} = 54,750 \text{ cls}}{(number of engine} \\ on/off cycles over 15 yr}$ of use) $\Delta T_{u} = 76^{\circ}C$ (average thermal cycle temperature change in use environment)	<u>Temperature</u> Cycling (TC)	$\underline{\Delta T_t = 205 \text{ °C}}$ <u>(thermal cycle</u> <u>temperature</u> <u>change in test</u> <u>environment:</u> <u>-55 °C to +150 °C</u> )	$\frac{Coffin \text{ Manson}}{A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m}$ <u>Also applicable for Power</u> <u>Temperature Cycle (PTC)</u>	<u>m = 4</u> (Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials)	$\frac{n_t = 1034 \text{ cls}}{(number of cycles)}$ $\frac{n_t = n_u}{A_f}$	<u>1000 cls</u>
	Humidity (Option 1)	$t_{u} = 131,400 \text{ hr}$ (average on/off time over 15 yr of use) $\frac{\text{RH}_{u} = 74\%}{(\text{average relative})}$ (average relative humidity in use environment) $T_{u} = 32^{\circ}\text{C}$ (average temperature in use environment: 9% @ 87^{\circ}\text{C} - time on and 91% @ 27^{\circ}\text{C} - time off)	<u>Temperature</u> <u>Humidity</u> <u>Bias</u> (THB)	$\frac{\text{RH}_{\text{t}} = 85\%}{(\text{relative humidity})}$ $\frac{\text{in test}}{\text{environment}}$ $\frac{\text{T}_{\text{t}} = 85 ^{\circ}\text{C}}{(\text{ambient})}$ $\frac{\text{test environment}}{\text{test environment}}$	$\frac{\text{Hallberg-Peck}}{A_{f} = \left(\frac{RH_{t}}{RH_{u}}\right)^{p} \cdot \exp\left[\frac{E_{u}}{k_{B}} \cdot \left(\frac{1}{T_{u}} - \frac{1}{T_{t}}\right)\right]}$ $\frac{\text{Also applicable for Highly}}{\text{Accelerated Steam Test (HAST)}}$ $\frac{\text{and Unbiased Humidity Steam Test}}{(\text{UHST}). \text{ See Notes.}}$	p = 3 <u>(Peck exponent, 3 is to be used</u> <u>for bond pad corrosion)</u> $E_a = 0.8 \text{ eV}$ <u>(activation energy; 0.8 eV is to be</u> <u>used for bond pad corrosion)</u> $k_B = 8.61733 \times 10^{-5} \text{ eV/K}$ <u>(Boltzmann's Constant)</u>	$\frac{\underline{T}_{t} = 960 \text{ hr}}{\underline{t}_{t} = \frac{t_{u}}{A_{f}}}$	<u>1000 hr</u>

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#### Table A7.1: Basic Calculations for AEC-Q100 Stress Test Conditions and Durations (continued)

<u>Loading</u>	Mission Profile Input	Stress Test	<u>Stress</u> Conditions	Acceleration Model (all temperatures in K, not in °C)	Model Parameters	Calculated Test Duration	Q100 Test Duration
<u>Humidity</u> (Option 2)	$\frac{t_u = 131,400 \text{ hr}}{(average on/off time} - over 15 \text{ yr of use})}$ $\frac{RH_u = 74\%}{(average relative} - humidity in use} - environment)$ $T_u = 32^{\circ}C - (average temperature} - in use environment:} - 9\% @ 87^{\circ}C - time on} - and 91\% @ 27^{\circ}C - time off)$	Highly Accelerated Steam Test (HAST)	$\frac{\text{RH}_{\text{t}} = 85\%}{(\text{relative})}$ $\frac{\text{humidity in test}}{\text{environment}}$ $\frac{\text{T}_{\text{t}} = 130^{\circ}\text{C}}{(\text{ambient})}$ $\frac{\text{T}_{\text{t}} = 130^{\circ}\text{C}}{\text{temperature in}}$	Hallberg-Peck $A_{f} = \left(\frac{RH_{t}}{RH_{u}}\right)^{p} \cdot \exp\left[\frac{E_{a}}{k_{B}} \cdot \left(\frac{1}{T_{u}} - \frac{1}{T_{t}}\right)\right]$ Also applicable for Temperature Humidity Bias (THB) and Unbiased Humidity Steam Test (UHST). See Notes.	$\frac{p = 3}{(Peck exponent, 3 is to be used}{for bond pad corrosion)}$ $\frac{E_a = 0.8 \text{ eV}}{(activation energy; 0.8 eV is to be}{used for bond pad corrosion)}$ $\frac{k_B = 8.61733 \times 10^{-5} \text{ eV/K}}{(Boltzmann's Constant)}$	$\frac{T_t = 53 \text{ hr}}{t_t = \frac{t_u}{A_f}}$	<u>96 hr</u>

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Notes:

- Autoclave (121 °C/100%RH) is a highly accelerated test using a saturated moisture condition that will tend to uncover failure mechanisms not seen in normal use conditions. For this reason, autoclave is not a test whose test conditions can be derived through models and assumptions. The current test conditions were selected decades ago and the test has been used as part of a standard qualification ever since.
- Most Pressure Pot testing is performed with an Al Pressure Pot. Air purging is done at 100 °C boiling water, and with both steam and liquid escaping from the vent. The chamber walls are not independently heated at all. Control of the chamber wall temperature; air purging procedure, during ramp-up; ramp-down temperature and pressure and overall temperature and pressure are key. In addition, when the test is ended the heater is turned off and the vent is opened. It takes about 3 minutes to fully vent the pot. A significant concern is that venting before the pot chamber drops to 100 °C, can cause a pressure differential from the >100 °C residual hot device and cause any water trapped in device void to create a pop-corning type of delamination.

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# **Revision History**

<u>Rev #</u>	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release.
A	May 19, 1995	Added copyright statement. Revised sections 2.3, 2.4.1, 2.4.4, 2.4.5, 2.8, 3.2 and 4.2, Tables 2, 3, 4 and Appendix 1, 2. Added Appendix 3.
В	Sept. 6, 1996	Revised sections 1.1, 1.2.3, 2.3, 3.1, and 3.2.1, Tables 2, 3, and 4, and Appendix 2.
С	Oct. 8, 1998	Revised sections 1.1, 1.1.3, 1.2.2, 2.2, 2.3, 2.4.2, 2.4.5, 2.6, 3.1, 3.2.1, 3.2.3, 2.3.4, 4.1, and 4.2, Tables 3 and 4, Appendix 2, and Appendix 3. Added section 1.1.1, Figures 1, 2, and 3, and Test Methods Q100-008 and -009. Deleted sections 2.7 and 2.8.
D	Aug. 25, 2000	Revised sections 1.1 and 2.3, Figures 2, 3, and 4, Tables 2, 3, and 4, Appendix 1, and Appendix 2. Added section 2.3.2, Test Methods Q100-010 and -011, and Figure 1.
Е	Jan. 31, 2001	Revised Figure 4.
F	July 18, 2003	Complete Revision.
G	May 14, 2007	Complete Revision. Revised document title to reflect that the stress test qualification requirements are failure mechanism based. Revised sections 1, 1.1, 1.2.1, 1.2.2, 1.2.3, 2.3.1, 2.4.4, 2.5, 3.2, 3.2.3, 4.2, and 4.3, Figure 2, Tables 2 and 3, Appendix 2, Appendix 4A, and Appendix 4B. Added sections 2.1.1, 3.1.1, Table 2 and 3 entries (test #D4, D5, E10, and E11), Appendix 6, and Test Method Q100-012. Deleted Table 2A.
Η	<u>Sept. 11, 2014</u>	Complete Revision. Revised sections 1.2.1, 1.3.1, 1.3.3, 2.2, 2.3.1, 2.3.3, 2.4.1, 2.4.5, 2.5, and 3.2.3, Figure 2, Tables 1 and 2, Appendix 1, Appendix 4A, Appendix 4B, and Revision History. Added Revision Summary, sections 1.2.4, 1.3.2, 1.3.4, 1.3.5, and 3.3, Table 2 and 3 entry (test #E12), Table 2 Legend (Note L), Tables A1.1 and A1.2, Appendix 7, Figures A7.1 and A7.2, and Table A7.1. Deleted section 3.1.1, Table 2 and 3 entries (test #E2 and E8).
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