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FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR DISCRETE OPTOELECTRONIC SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS

Automotive Electronics Council
Component Technical Committee

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Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document: (in alphabetical order)

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Component Technical Committee

FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR DISCRETE OPTOELECTRONIC SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS

Unless otherwise stated herein, the date of implementation of this standard for new qualifications and re-qualifications is as of the publish date above.

1. SCOPE

This document defines the minimum stress test driven qualification requirements and references test conditions for qualification of discrete optoelectronic semiconductors (e.g., light emitting diodes, photodiodes, laser components (see Figure 1)) in all exterior and interior automotive application. It combines state of the art qualification testing, documented in various norms (e.g., JEDEC, IEC, MIL-STD) and manufacturer qualification standards.

For the qualification of parts using optoelectronic functions together with other components (e.g., multichip modules with sensors and integrated signal processing, solid state relays, LEDs mounted on boards with additional mechanical connectors, etc.), it is mandatory to combine tests defined in this specification with further tests described in other adequate (AEC) norms.

This document does not relieve the supplier of their responsibility to meet their own company's internal qualification program. Additionally, this document does not relieve the supplier from meeting any user requirements outside the scope of this document. In this document, "user" is defined as any company developing or using a discrete optoelectronic semiconductor part in production. The user is responsible to confirm and validate all qualification and assessment data that substantiates conformance to this document.

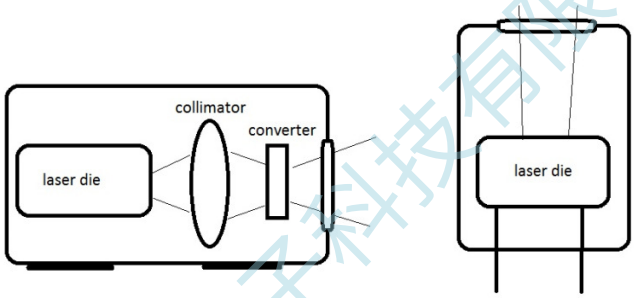


Figure 1: Examples of Laser Components

Note: The term “laser component” within this norm includes an assembled singular pure laser die as well as an assembled combination of laser die, collimator, and converter.

1.1 Purpose

The purpose of this specification is to determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality / reliability in the application.

1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

1.2.1 Automotive

AEC-Q001 Guidelines for Part Average Testing
AEC-Q002 Guidelines for Statistical Yield Analysis
AEC-Q005 Pb-Free Test Requirements
SAE/USCAR-33 Specification for testing LED Modules
The following documents from AEC-Q101 are respectively valid also for qualification of discrete optoelectronic semiconductors according to AEC-Q102:

AEC-Q101-001: Electrostatic Discharge Test - Human Body Model
AEC-Q101-003: Wire Bond Shear Test
AEC-Q101-005: Electrostatic Discharge Test – Charged Device Model

1.2.2 Industrial

JEDEC JESD-22 Reliability Test Methods for Packaged Devices
J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.
J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
JESD51-50 Overview of Methodologies for the Thermal Measurement of Single- and Multi-Chip Single- and Multi-PN Junction Light-Emitting Diodes (LEDs)
JESD51-51 Implementation of the Electrical Test Method for the Measurement of Real Thermal Resistance and Impedance of Light-Emitting Diodes with Exposed Cooling
JESD51-52 Guidelines for Combining CIE 127-2007 Total Flux Measurements with Thermal Measurements of LEDs with Exposed Cooling Surface
ANSI/ESDA/JEDEC JS-001 Human Body Model (HBM) - Component Level
IEC 600068-2-43 Hydrogen sulphide test for contacts and connections
IEC 600068-2-60 Flowing mixed gas corrosion test

1.2.3 Military

MIL-STD-750-1 Environmental Test Methods for Semiconductor Devices
MIL-STD-750-2 Mechanical Test Methods for Semiconductor Devices

1.2.4 Other

QS-9000
ISO-TS-16949

1.3 Definitions

1.3.1 AEC-Q102 Qualification

Successful completion and documentation of the test results from requirements outlined in this document allows the supplier to claim that the part is “AEC-Q102 qualified”. The supplier, in agreement with the user, can perform qualification at sample sizes and conditions less stringent than what this document requires. However, that part cannot be considered “AEC-Q102 qualified” until such time that the unfulfilled requirements have been successfully completed.

For ESD, it is highly recommended that the passing voltage be specified in the supplier datasheet with a footnote on any pin exceptions. This will allow suppliers to state, for example, "AEC-Q102 qualified to ESD H1B", implying that supplier passes all AEC tests except the ESD level. Note that there are no "certifications" for AEC-Q102 qualification and there is no certification board run by AEC to qualify parts.

The minimum temperature range for discrete optoelectronic semiconductors per this specification shall be -40°C up to the maximum operating temperature defined in the part specification.

1.3.2 Approval for Use in an Application

"Approval" is defined as user approval for use of a part in their application. The user's method of approval is beyond the scope of this document.

1.3.3 Terminology

In this document, "part" refers to the same entity as would "device" or "component" that is a singulated light emitting diode, photo diode, photo transistor, etc., that can be designed in various ways, sometimes using an integrated protection device for electrostatic discharge (e.g., ESD-diode).

2. GENERAL REQUIREMENTS

2.1 Precedence of Requirements

In the event of conflict in the requirements of this specification and those of any other documents, the following order of precedence applies:

a. The purchase order
b. The individual agreed upon part specification
c. This document
d. The reference documents in Section 1.2 of this document
e. The supplier's data sheet

For the part to be considered qualified per this specification, the purchase order and/or individual part specification cannot waive or detract from the requirements of this document.

2.2 The Use of Generic Data to Satisfy Qualification and Re-qualification Requirements

The use of generic (family) data to simplify the qualification/re-qualification process is encouraged. To be considered, the generic data must be based on the following criteria:

a. Part qualification requirements listed in Table 2.
b. Matrix of specific requirements associated with each characteristic of the part and manufacturing process as shown in Table 3a-c.
c. Definition of family guidelines established in Appendix 1.
d. Represent a random sample of the normal population.

Appendix 1 defines the criteria by which parts are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable to the qualification of the part in question.

With proper attention to these qualification family guidelines, information applicable to other parts in the family can be accumulated. This information can be used to demonstrate generic reliability of a part family and minimize the need for part-specific qualification test programs. This can be achieved through qualification of a range of parts representing the "four corners" of the qualification family (e.g., highest/lowest current, minimum/maximum amount of dies, etc.). Sources of generic data should come from supplier-certified test labs, and can include internal supplier's qualifications, user-specific qualifications and supplier's in-process monitors. The generic data to be submitted must meet or exceed the test conditions, sample size and number of lots specified in Table 2.

Table 1 provides guidelines showing how the available part test data may be applied to reducing the number of lots required for qualification. Electrical characterization to the individual user part

specification must be performed for each part submission, generic characterization data is not allowed. Whenever appropriate generic data can be used, the supplier has to give a rationale to the user(s). **The user(s) will be the final authority on the acceptance of generic data in lieu of specific part test data.**

Part Information	Lot Requirements for Qualification
New part, no applicable generic data.	Lot and sample size requirements per Table 2.
A part in a family is qualified. The part to be qualified is less complex and meets the Family Qualification Definition per Appendix 1.	Only part specific tests as defined in Section 4.2 are required. Lot and sample size requirements per Table 2 for the required tests.
A new part that has some applicable generic data.	Review Appendix 1 to determine required tests from Table 2. Lot and sample sizes per Table 2 for the required tests.
Part process change.	Review Tables 3a-c to determine which tests from Table 2 should be considered. Lot and sample sizes per Table 2 for the required tests.
Qualification/Requalification involving multiple sites or families	Refer to Appendix 1, Section 3.

Table 1: Part Qualification/Re-qualification Lot Requirements

Table 2 defines a set of qualification tests that must be considered for both new part qualifications and re-qualification associated with a design or process change.

Tables 3a-c define a matrix of appropriate qualification tests that must be considered for any changes proposed for the part. Tables 3a-c are the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and user should use as a baseline for discussion of tests that are required for the qualification/requalification in question. **It is the supplier's responsibility to present and document rationale for why any of the highlighted tests need not be performed.**

2.3 Test Samples

2.3.1 Lot Requirements

Lot requirements are designated in Table 2, herein.

2.3.2 Production Requirements

All qualification parts shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at projected production volumes.

2.3.3 Reusability of Test Samples

Parts that have been used for nondestructive qualification tests may be used to populate other qualification tests. Parts that have been used for destructive qualification tests may not be used any further except for engineering analysis.

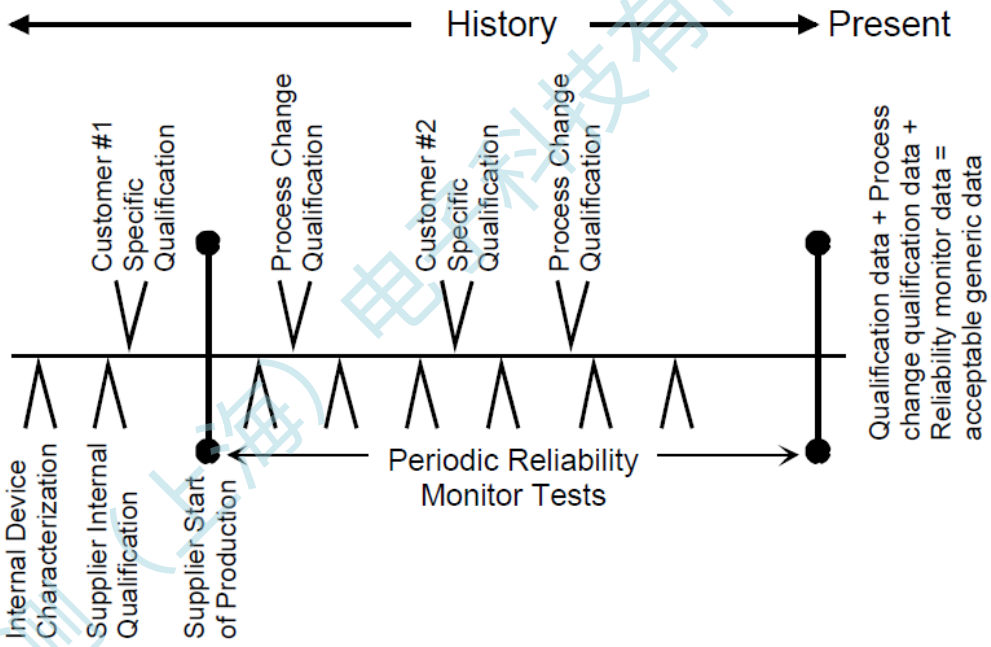
2.3.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 2. If the supplier elects to submit generic data for qualification/requalification, the specific test conditions and results must be reported. Existing applicable generic data should first be used to satisfy these requirements and those of Section 2.2 for each test requirement in Table 2. Part specific qualification testing should be performed if the generic data does not satisfy these requirements.

The supplier must perform any combination of the specific part to be qualified and/or an acceptable generic part(s) that totals a minimum of pieces as defined in Table 2.

2.3.5 Time Limit for Acceptance of Generic Data

There are no time limits for the acceptability of generic data as long as the appropriate reliability data is submitted to the user for evaluation. Use the diagram below for appropriate sources of reliability data that can be used. This data must come from the specific part or a part in the same qualification family, as defined in Appendix 1. Potential sources of data could include any customer specific data (withhold customer name), process change qualification, and periodic reliability monitor data (see Figure 2).



Note: Some process changes may affect the use of generic data such that data obtained before these types of changes will not be acceptable for use as generic data.

Figure 2: Generic Data Time Line

2.3.6 Assembly on Test Boards

If the parts have to be mounted on test boards, the supplier shall make an appropriate choice of process and materials, which shall be documented in the test report.

It is recommended to prove the quality of the interconnection by adequate methods (e.g., X-ray, Rth measurement, Vf measurement, etc.) prior to stress testing.

2.3.7 Pre- and Post-Stress Test Requirements

Electrical and optical parameters as defined in Appendix 5 have to be measured before and after the stress testing at the nominal test conditions as mentioned in the appropriate part specification. For LEDs and laser components the forward voltage has to be measured also at the minimum (or lower) and maximum specified drive current. If no minimum drive current is specified, 10% of the nominal current should be chosen.

All pre- and post-stress test parts must be tested to the electrical characteristics defined in the individual user part detail specification at room temperature.

In addition, a simple functioning/no functioning test (e.g., LEDs: light/no light) at minimum and maximum allowed temperature according to the manufacturer datasheet is mandatory for certain stress tests (see Table 2 – Additional Requirements). Alternatively, a failure detection during stress testing is possible.

2.4 Definition of Test Failure after Stressing

Test failures are defined as devices exhibiting any of the following criteria:

a. Parts not meeting the electrical and optical test limits defined in the first user's part specification or appropriate supplier generic part specification. Minimum test parametric requirements shall be as specified in Appendix 5.

b. Parts not remaining within ± x% (as defined in Appendix 5) of the initial reading of each test after completion of environmental testing. Parts exceeding these requirements must be justified by the supplier and approved by the user. For leakages below 100nA, tester accuracy may prevent a post stress analysis to initial reading.

c. Any part exhibiting physical damage attributable to the environmental test (migration, corrosion, mechanical damage, delamination, other). Note that some physical damage may mutually be agreed by supplier and customer as only cosmetic defect with no effect on the qualification result.

If the cause of failure is agreed (by the manufacturer and the user) to be due to mishandling, interconnect to the test board, ESD or some other cause unrelated to the test conditions, the failure shall be discounted, but reported as part of the data submission.

2.5 Criteria for Passing Qualification/Re-qualification

Passing all appropriate qualification tests specified in Table 2, either by performing the tests (acceptance of zero failures using the specified minimum sample size) on the specific part or demonstrating acceptable family generic data (using the family definition guidelines defined in Appendix 1 and the total required lot and sample sizes), qualifies the part per this document.

Parts that have failed the acceptance criteria of tests required by this document require the supplier to satisfactorily determine root cause and corrective action to assure the user that the failure mechanism is understood and contained. The part shall not be considered as passing stress-test qualification until the root cause of the failure is determined and the corrective and preventive actions are confirmed to be effective. New samples or data may be requested to verify the corrective action. If generic data contains any failures, the data is not usable as generic data unless the supplier has documented corrective action or containment for the failure condition.

Any unique reliability tests or conditions requested by the user and not specified in this document shall be agreed upon between the supplier and user requesting the test, and will not preclude a device from passing stress-test qualification as defined by this document.

2.6 Alternative Testing Requirements

Any deviation from the test requirements and conditions listed in Table 2 are beyond the scope of this document. Deviations (e.g., accelerated test methods) must be demonstrated to the AEC for consideration and inclusion into future revisions of this document.

See Appendix 7: Guideline on Relationship of Robustness Validation to AEC-Q102 for more information.

2.7 Temperature Measuring Position

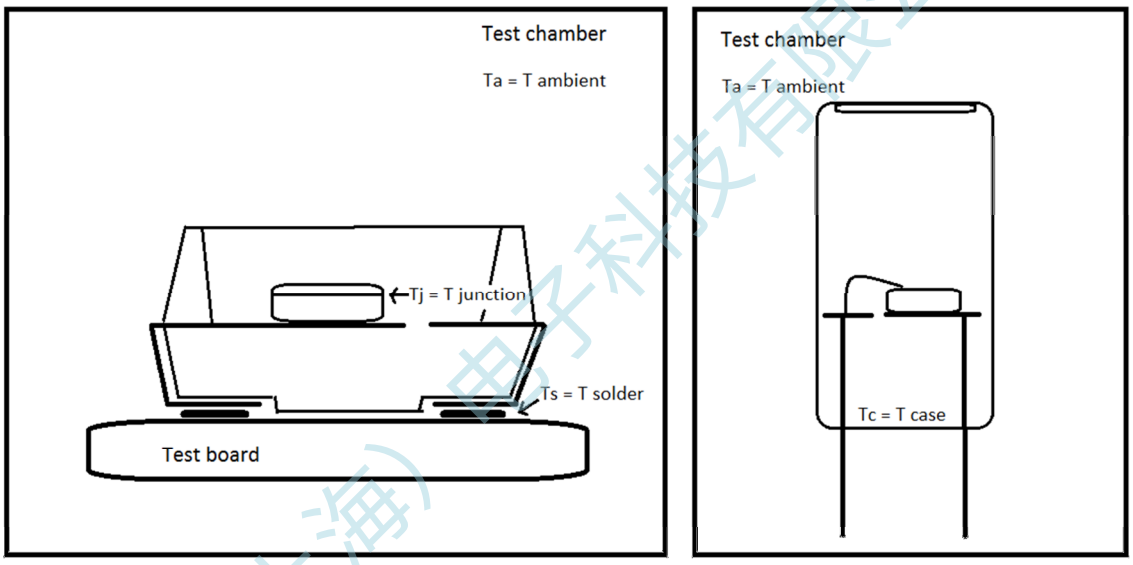


Figure 3: Definition of $T_{ambient}$, T_{solder}, T_{case} and $T_{junction}$. For different LED designs, the definition of the measuring points must be done respectively.

For SMD parts, T_{solder} is defined as the temperature measured at the hottest solder connection between the part and the board used for assembly. For some parts types like “Chip on Board LED” or leaded laser components, other assembly methods like screwing or clinching are used. In this case, T_{solder} can be replaced by T_{case} measured at an appropriate position of the part. Supplier has to define and provide the used definition.

3. QUALIFICATION AND REQUALIFICATION

3.1 Qualification of a New Part

Stress test requirements and corresponding test conditions for a new part qualification are listed in Table 2. For each qualification, the supplier must present data for ALL of these tests (see Appendix 4), whether it is stress test results on the specific part or acceptable generic family data. A review is to be made of other parts in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the user. For each part qualification, the supplier must also present a Certificate of Design, Construction and Qualification to the requesting user. See Appendix 2.

3.2 Re-qualification of a Changed Part

Re-qualification of a part is required when the supplier makes a change to the product and/or process that impacts (or could potentially impact) the form, fit, function, quality and/or reliability of the part (see Tables 3a-c for guidelines).

3.2.1 Process Change Notification

The supplier will meet mutually agreed upon requirements for product/process changes.

3.2.2 Changes Requiring Re-qualification

As a minimum, any change to the product, as defined above, requires performing the applicable tests listed in Table 2, using Tables 3a-c to determine the re-qualification test plan. Tables 3a-c should be used as a guide for determining which tests need to be performed or whether equivalent generic data can be submitted for the test(s).

3.2.3 Criteria for Passing Requalification

All requalification failures shall be analyzed for root cause, with corrective and preventive actions established as required. The part and/or qualification family may be granted “qualification status” if, as a minimum, proper containment is demonstrated and approved by the user, until corrective and preventative actions are in place.

3.2.4 User Approval

A change may not affect a part’s specification, but may affect its performance in an application. Individual user authorization of a process change shall be based on a contract between supplier and user, and is outside the scope of this document.

3.3 Qualification Test Plan

The supplier is requested to initiate a discussion with each user (as needed) resulting in completion of a signed Qualification Test Plan agreement as soon as possible after supplier selection for new parts, and at the time of notification (see Section 3.2.2) prior to process changes. The Qualification Test Plan, as defined in Appendix 3, shall be used to provide a consistent method of documentation supporting what testing will be performed as required by Tables 2 & 3a-c.

4 QUALIFICATION TESTS

4.1 General Tests

Test details are given in Table 2. Not all tests apply to all parts. For example, certain tests apply only to uncasted parts. The applicable tests for the particular part type are indicated in the "Note" column and the "Additional Requirements" column of Table 2. The "Additional Requirements" column of Table 2 also serves to highlight test requirements that supersede those described in the referenced test. Any unique qualification tests or conditions requested by the user and not specified in this document shall be negotiated between the supplier and user requesting the test.

4.2 Part Specific Tests

The following tests must be performed on the specific part (i.e., family data is not allowed for these tests):

a. Electrostatic Discharge Characterization (Table 2, Test #10a & b)

b. Parametric Verification (Table 2, Test #4) - The supplier must demonstrate that the part is capable of meeting parametric limits detailed in the individual user part specification.

4.3 Data Submission Format

A data summary shall be submitted as defined in Appendix 4. Raw data with a graphical presentation shall be submitted to the individual user upon request. **All data and documents (e.g., justification for non-performed tests, etc.) shall be maintained by the supplier in accordance with QS-9000 and/or TS-16949 requirements.**

4.4 Requirements for Testing Pb-free Components

The supplier shall follow the requirements of AEC-Q005 Pb-Free Test Requirements for all parts whose plating material on the leads/terminations contains <1000ppm by weight of lead (Pb).

TABLE 2 - QUALIFICATION TEST DEFINITIONS

#	STRESS	ABV	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD (current revision)	ADDITIONAL REQUIREMENTS
1	**Pre- and Post-Stress Electrical and Photometric Test**	**TEST**	N, G	All qualification parts tested per the requirements of the appropriate part specification.		0	User specification or supplier's standard specification	Test is performed as specified in the applicable stress reference. See also Section 2.3.7.
2	**Pre-conditioning**	**PC**	G, S	SMD qualification parts at least before Test #6, #7, & #8		0	JEDEC JESD22-A113	Performed on surface mount parts (SMDs) at least prior to Test #6, #7 & #8. Where applicable, preconditioning level and Peak Reflow Temperature must be reported when preconditioning and/or MSL is performed. Any replacement of parts must be reported. **TEST before and after PC.**
3	**External Visual**	**EV**	N, G	All qualification parts submitted for testing except DPA and PD		0	JEDEC JESD22-B101	Inspect part construction, marking and workmanship.
4	**Parametric Verification**	**PV**	N	25	3 Note A	0	Individual AEC user specification	Test all parameters according to user specification over the part temperature range to insure specification compliance.
5a	**High Temperature Operating Life HTOL**	**HTOL1**	D, G, X, Y	26	3 Note B	0	JEDEC JESD22-A108	**Only for LED and Laser Component.** Duration 1000 h at maximum specified T_{solder}. Choose corresponding drive current according to derating curve to achieve max Tj defined in the part specification. Test 5a is equivalent to 5b if no derating. For use within special application; a longer test duration may be needed to ensure reliability over application lifetime. For details, see Appendix 7a "Reliability Validation for LEDs". **TEST before and after HTOL1.**
5b	**High Temperature Operating Life HTOL**	**HTOL2**	D, G, X, Y	26	3 Note B	0	JEDEC JESD22-A108	**Only for LED and Laser Component** Duration 1000 h at maximum specified drive current. Choose corresponding T_{solder} according to derating curve to achieve max Tj defined in the part specification. Test 5b is equivalent to 5a if no derating. For use within special application; a longer test duration may be needed to ensure reliability over application lifetime. For details, see Appendix 7a "Reliability Validation for LEDs". **TEST before and after HTOL2.**

TABLE 2 - QUALIFICATION TEST DEFINITIONS (CONTINUED)

#	STRESS	ABV	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD (current revision)	ADDITIONAL REQUIREMENTS
5c	**High Temperature Reverse Bias**	**HTRB**	D, G, Z	26	3 Note B	0	JEDEC JESD22-A108	**Only for Photodiodes and Phototransistors.** Duration 1000 h at maximum specified T_{solder} Operated with continuous reverse bias Photodiodes: Vr = maximum rated reverse voltage defined in part specification: Phototransistors: Vce = maximum rated collector emitter voltage defined in part specification. No light exposure. **TEST before and after HTRB.**
6a	**Wet High Temperature Operating Life**	**WHTOL 1**	D, G, X, Y	26	3 Note B	0	JEDEC JESD22-A101	**Only for LED and Laser Component.** **PC before WHTOL1.** Duration 1000 h at T_{solder} = 85 °C / 85% RH with drive current according to derating curve to achieve max Tj defined in the part specification. Operated with power cycle 30 min on / 30 min off. **TEST before and after WHTOL1. DPA after WHTOL1.**
6b	**Wet High Temperature Operating Life**	**WHTOL 2**	D, G, X, Y	26	3 Note B	0	JEDEC JESD22-A101	**Only for LED and Laser Component** **PC before WHTOL2** Duration 1000 h at T_{solder} = 85 °C / 85% RH with minimum drive current according to part specification. If no minimum rated drive current is specified, a drive current shall be chosen not to exceed a rise of 3 K for $T_{junction}$. **TEST before and after WHTOL2. DPA after WHTOL2.**
6c	**High Humidity High Temperature Reverse Bias**	**H³TRB**	D, G, Z	26	3 Note B	0	JEDEC JESD22-A101	**Only for Photodiodes and Phototransistors.** **PC before H³TRB.** Duration 1000 h at T_{solder} = 85 °C 85% RH operated with continues reverse bias: Photodiodes: Vr = 0.8x maximum rated reverse voltage defined in part specification: Phototransistors: Vce = 0.8x maximum rated collector emitter voltage defined in part specification: Maximum specified power dissipation according to derating curve. No light exposure. **TEST before and after H³TRB. DPA after H³TRB.**

TABLE 2 - QUALIFICATION TEST DEFINITIONS (CONTINUED)

#	STRESS	ABV	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD (current revision)	ADDITIONAL REQUIREMENTS
7	**Temperature Cycling**	**TC**	D, G	26	3 Note B	0	JEDEC JESD22-A104	**PC before TC.** Duration 1000 cycles. Minimum soak & dwell time 15 min. Minimum temperature as specified in part specification. Choose TC condition exceeding or equal to the operating temperature according to the appropriate part specification: TC condition 1: *max* T_{solder} = 85 °C TC condition 2: *max* T_{solder} = 100 °C TC condition 3: *max* T_{solder} = 110 °C TC condition 4: *max* T_{solder} = 125 °C TC condition and transfer time shall be mentioned in the test report. It is recommended to decapsulate the part after TC and perform WBP if applicable. Report data. The supplier has to provide explanation in case that WBP cannot be performed. **TEST before and after TC.**
8a	**Power Temperature Cycling**	**PTC**	D, G, X, Y	26	3 Note B	0	JEDEC JESD22-A105	**Only for LED and Laser Component.** **PC before PTC.** Duration 1000 temperature cycles with drive current according to derating curve to achieve max Tj specified in part specification. Operated with power cycle 5 min on / 5 min off. Minimum temperature as specified in part specification. For maximum temperature choose: PTC condition 1: *max* T_{solder} = 85 °C PTC condition 2: *max* T_{solder} = 105 °C PTC condition 3: *max* T_{solder} = 125 °C PTC condition should be chosen closest to the operating temperature range within the appropriate part specification. PTC condition shall be mentioned in the test report. For use within special application; a longer test duration may be needed to ensure reliability over application lifetime. For details, see Appendix 7a “Reliability Validation for LEDs”. **TEST before and after PTC. DPA after PTC.**

TABLE 2 - QUALIFICATION TEST DEFINITIONS (CONTINUED)

#	STRESS	ABV	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD (current revision)	ADDITIONAL REQUIREMENTS
8b	**Intermittent Operational Life**	**IOL**	D, G, Z	26	3 Note B	0	MIL-STD-750-1 Method 1037	**Only for Photodiodes and Phototransistors.** Only to be performed if enough power can be generated to achieve $\Delta T_J \geq 60$ °C. $T_{ambient}$ = 25 °C. Parts powered but not to exceed absolute maximum ratings. Number of cycles required: 60000/(x+y) with: x = the minimum amount of minutes it takes for the part to reach the required ΔT_J from ambient temperature. y = the minimum amount of minutes it takes for the part to cool to ambient temperature from required ΔT_J. **TEST before and after IOL. DPA after IOL.**
9	**Low Temperature Operating Life**	**LTOL**	D, G, X	26	3 Note B	0	JEDEC JESD22-A108	**Only for Laser Component.** Duration 1000 h at T_{solder} = min. with maximum drive current according to derating curve defined in the part specification. Operated with power cycle 30 min on / 30 min off.
10a	**Electrostatic Discharge Human Body Model**	**HBM**	D	10	3	0	ANSI/ESDA/JEDEC JS-001	**TEST before and after HBM.**
10b	**Electrostatic Discharge Charged Device Model**	**CDM**	D, 1	10	3	0	AEC Q101-005	CDM may not be applicable for some packages. For more details, see Note 1. **TEST before and after CDM.**
11	**Destructive Physical Analysis**	**DPA**	D, G	2 (for each test)	1 Note B	0	Appendix 6	Random sample of parts that have successfully completed PTC/IOL, WHTOL/H³TRB, H2S, and FMG. (2 samples each)
12	**Physical Dimension**	**PD**	N, G	10	3	0	JEDEC JESD22-B100	Verify physical dimensions to the applicable user part packaging specification for dimensions and tolerances.
13	**Terminal Strength**	**TS**	D, G, L	10	3	0	MIL-STD-750-2 Method 2036	Evaluate lead integrity of leaded parts only.

TABLE 2 - QUALIFICATION TEST DEFINITIONS (CONTINUED)

#	STRESS	ABV	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD (current revision)	ADDITIONAL REQUIREMENTS
14	**Constant Acceleration**	**CA**	D, G, U, X (seq1)	10	3 Note B	0	MIL-STD-750-2 Method 2006	**Only for Laser Component.** Y1 plane only, 15000 g-force. **TEST before and after CA.**
15	**Vibration Variable Frequency**	**VVF**	D, G, U (seq2)	Items 14 through 17 are sequential tests (seq1 to seq4) for uncasted packages (See Note U and H)		0	JEDEC JESD22-B103	Use a constant displacement of 1.5 mm (double amplitude) over the range of 20 Hz to 100Hz and a 200 m/s² constant peak acceleration over the range of 100 Hz to 2 kHz. **TEST before and after VVF.**
16	**Mechanical Shock**	**MS**	D, G, U (seq3)			0	JEDEC JESD22-B104	1500 g's for 0.5 ms, 5 blows, 3 orientations. **TEST before and after MS.**
17	**Hermeticity**	**HER**	D, G, H, X (seq4)			0	JEDEC JESD22-A109	**Only for Laser Component.** Fine and Gross leak test per individual user specification.
18 A	**Resistance to Solder Heat**	**RSH (-reflow)**	D, G	10	3	0	Lead containing devices: JEDEC JESD22-A113 J-STD-020 Lead (Pb)-free devices: AEC-Q005	Only applicable if the supplier declared the part to be solderable by reflow soldering. Reflow soldering 3 times at peak reflow temperature, defined in J-STD-020. **TEST before and after RSH.**
18b	**Resistance to Solder Heat**	**RSH (-wave)**	D, G	10	3	0	Lead containing devices: JESD22-B106 Lead (Pb)-free devices: AEC-Q005	Only applicable if the supplier declared the part to be solderable by wave soldering. **TEST before and after RSH.**

TABLE 2 - QUALIFICATION TEST DEFINITIONS (CONTINUED)								
#	STRESS	ABV	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD (current revision)	ADDITIONAL REQUIREMENTS
19	**Solderability**	**SD**	D, G	10	3 Note B	0	Lead containing devices: JEDEC J-STD-002 JESD22-B102 Lead (Pb)-free devices: AEC-Q005	Magnification 50x. Reference solder conditions in Table 2A. Apply test method A for through-hole, or both test methods B and D for SMD.
20	**Pulsed Operating Life**	**PLT**	D, G, X, Y	26	3	0	JEDEC JESD22-A108	**Only for LED and Laser.** Duration 1000 h at T_{solder} = 55 °C. Operated with pulse width 100 µs and duty cycle 3%. Maximum pulse height according to part's specification. **TEST before and after PLT.**
21	**Dew**	**DEW**	D, G	26	3	0	JEDEC JESD22-A100	T cycling 30-65 °C with dwell time at 65 °C between 4-8 h, transition time between 2-4 h; RH = 90-98%. Duration 1008 h with minimum drive current according to part specification. If no minimum rated drive current is specified, a drive current shall be chosen not to exceed a rise of 3 K for $T_{junction}$. **TEST before and after DEW.**
22	**Hydrogen Sulphide**	**H2S**	D, G	26	3	0	IEC 60068-2-43	Duration 336 h at 40 °C and 90% RH. H_2S concentration: 15 x 10^{-6} **TEST before and after H2S. DPA after H2S.**
23	**Flowing Mixed Gas**	**FMG**	D, G	26	3	0	IEC 60068-2-60 Test method 4	**Duration** 500 h at 25 °C and 75% RH. H_2S concentration: 10 x 10^{-9} SO_2 concentration: 200 x 10^{-9} NO_2 concentration: 200 x 10^{-9} Cl_2 concentration: 10 x 10^{-9} **TEST before and after FMG. DPA after FMG.**

TABLE 2 - QUALIFICATION TEST DEFINITIONS (CONTINUED)								
#	STRESS	ABV	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD (current revision)	ADDITIONAL REQUIREMENTS
24	**Thermal Resistance**	**TR**	D, G, X, Y	10 each, pre- & post-change	1	0	JEDEC JESD51-50 JESD51-51 JESD51-52	Measure thermal resistance according to JESD51-50, JESD51-51, and JESD51-52 to assure specification compliance.
25	**Wire Bond Pull**	**WBP**	D, G, W, E	10 bonds from min of 5 parts	3	0	MIL-STD-750-2 Method 2037	Pre- & Post-process change comparison to evaluate process change robustness. Data may be provided within PPAP (C_{pk} > 1.67).
26	**Wire Bond Shear**	**WBS**	D, G, W, E	10 bonds from min of 5 parts	3	0	AEC Q101-003	Pre- & Post-process change comparison to evaluate process change robustness. Data may be provided within PPAP (C_{pk} > 1.67).
27	**Die Shear**	**DS**	D, G	5	3	0	MIL-STD-750-2 Method 2017	Pre- & Post-process change comparison to evaluate process change robustness. Data may be provided within PPAP (C_{pk} > 1.67).
28	**Whisker Growth**	**WG**	G	see test method	see test method	see test method	AEC-Q005	**Only for parts with Sn-based lead finishes.** Test to be done on a family basis (plating metallization, lead configuration).

LEGEND FOR TABLE 2

Notes:

- A For parametric verification data, sometimes circumstances may necessitate the acceptance of only one lot by the user. Should a subsequent user decide to use a previous user's qualification approval, it will be the subsequent user's responsibility to verify an acceptable number of lots were used.
- B Where generic (family) data is provided in lieu of component specific data, 3 lots are required.
- D Destructive test, parts are not to be reused for qualification or production.
- E Ensure that each size wire is represented in the sample size.
- G Generic data allowed. See Section 2.2.
- L Required for leaded parts only.
- N Nondestructive test, parts can be used to populate other tests or they can be used for production.
- P Only for parts with Sn-based lead finishes.
- S Required for surface mount parts only.
- U Required only for uncasted parts. Items #14 through #17 are performed as a sequential test to evaluate mechanical integrity of packages containing internal cavities. Number in parentheses below notes indicates sequence.
- H Required for hermetic packaged parts only. Items #14 through #17 are performed as a sequential test to evaluate mechanical integrity of packages containing internal cavities. Number in parentheses below notes indicates sequence.
- W Required only for parts using internal wire bonds.
- X Required only for Laser components.
- Y Required only for LED.
- Z Required only for Photodiodes and Phototransistors.
- 1 Small package consideration for CDM testing:
  CDM testing of small packages is very challenging. The vacuum used to hold the package in place during testing is not effective when the package is under a few square millimeters. (The same may apply for round shape parts.) The capacitance between the device under test and the field plate is also very small, which results in very fast CDM current pulses. These pulses have non-negligible peak currents, but have very fast rise times and very narrow pulse widths, making the pulses impossible to measure with standard 1 GHz measurement systems. Additionally, the total charge within the pulses is so small that CDM failures of semiconductors in very small packages have seldom been seen. For these reasons, the testing of very small packages is often not performed (as agreed between supplier and customer) due to the difficulty of testing and the very low chance of failure. Any device or package that could not be completely CDM stressed due to package size shall be recorded.

Table 2A: Solderability Requirements (Test #19) for SnPb Plated Terminations

Type	Test Method	Solder Temperature	Steam Age Category	Exception for Dry Heat
Leaded Through-Hole	A	235°C	3	----------
SMD Standard Process	B	235°C	3	----------
SMD Low Temperature Solder	B	215°C	--	4hrs @ 155ºC (in lieu of steam age)
SMD Dissolution of Metals test	D	260°C	3	----------

*** Note:** Refer to AEC-Q005 Pb-Free Test Requirements for solderability requirements of Pb-free terminated parts.

Tables 3a-c: Process Change Guidelines for the Selection of Tests

Tables 3a-c are based on the ZVEI "Guideline for Customer Notifications of Product and/or Process Changes (PCN) of Electronic Components specified for Automotive Applications" (DeQuMa), combined with Table 2 of this AEC-Q102 document.

Destructive Physical Analysis (see Appendix 6) has to be done after PTC/IOL, WHTOL / H³TRB, H2S, and FMG.

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change.

LEGEND FOR TABLES 3a-c

A Not applicable for Ag plated devices (Ag intended to fail for this test)
B Only if bond area/wirebond is changed/affected
C Only if dopant/implantation material is changed
D Only if dimensions are changing
E Only if min/max values are changing
F Sequence change only
H Non epoxy casted devices only
J Only for chip technology using wafer bonding
K Not applicable for Au plated devices
L Only if leadframe/substrate dimensions are changed
M Only if metal composition is changed including sequence
N Only for glued chips
O Only if process is changing
P Only if material properties are changed
Q Only if glue components are changing
R Only if marking technology changes
S Only if floor life is affected
T Only if board reliability is affected
U Only if underfill is affected
V Only for non-hermetic devices
W Only if risk of corrosion is increasing
Y Only for layer technology
Z Only if conversion technology changes
1 Only if data sheet parameters are affected
2 Only if outer dimensions are critical
3 Only for leaded parts
4 Only for hermetic parts

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Table 3a: Process Change Guideline for LEDs

Table 2 test number	5 ab	6 ab	7	8a	10 ab	12	13	15	16	18 ab	19	20	21	22	23	24	25	26	27	28			
Name of test / Type of change	High Temperature Operating Life	Wet High temperatur Operating Life	Temperature Cycling	Power Temperature Cycling	ESD Characterization	Physical Dimensions	Terminal Strenght	Vibration Variable Frequency	Mechanical Shock	Resist. to Solder Heat	Solderability	Pulse Life Test	Dew Test	Hydrogen Sulphide	Flow Mixed Gas Corosion	Thermal Resistance	Wire Bond Strength	Wire Bond Shear	Die Shear	Leadfree	Thermal Shock (for Robustness Validation only)	Parameter-Analysis: Comparison of current with changed	Remarks
	HTOL	WHTOL	TC	PTC	HBM/CDM	PD	TS	VVF	MS	RSH	SD	PLT	DEW	H2S	FMG	TR	WBP	WBS	DS	LF	TSK	PA	
ANY																							
Any change with impact on agreed upon contractual agreements																							
Any change with impact on technical interface or processability/manufacturabiliy of customer			T							S,T													
DATA SHEET																							
Change of datasheet parameters/electrical specification (min./max./typ. values) and/or Pulse/DC specification	E	E	E		E					S		E				E						E	
Correction of data sheet																							
Specification of additional parameters																						•	Formalism since this is not a product change, any addtional information.
DESIGN																							
Design changes in epitaxy.	•	•	-	•	•							•	H									•	
Design changes in routing/layout.	•	•	•	•						•		•	M	M	M		B	B	D,M		B, D,M	•	TR might be considered for complex die bond technologies
Die shrink	•	•	•	•	•					•		•				•	B	B	•			•	
LED package (except leadframe)	•	•	•	•		•	3	V	V	•	T		D	D	D	L	B	B	D			•	
Design of leadframe	•	•	•	•	•	•	3	V	V	•	T					•	B	B	D	2	•	•	
PROCESS - WAFER PRODUCTION																							
New / change of wafer substrate or carrier material	•	P	P	•	P					•		•	P	P	P	•			•		P	•	
Wafer diameter	•	•			P					•		•				•						•	
New final wafer thickness	•	P	•	•	P							•				•	B	B	•			•	
Change of electrically active doping/implantation element	•	C		C	•							•				•						•	
Change of stacking	•	•	F	•	•							•	F									•	
New / change of metallization (specifically chip frontside)	•	•	•	•	M,B							•	M	M	M		•	•			B	•	
New / change of metallization (specifically chip backside)	•	•	•	•	D,M					•		•	D,M	D,M	D,M	D,M			•		D,M	•	
Change in process technique (e.g. significant process changes like lithography, etch, oxide deposition, die back surface preparation/backgrind, ...)	Qualification effort depends on type of change.																						
Process Integrity: Tuning within specification																							
Change of material supplier with no impact on agreed specifications	Qualification effort depends on type of change.																						
Change of specified wafer process sequence (deletion and/or add. process step)	Qualification effort depends on type of change. PPAP has to be updated.																						
Change in die coating or passivaton	•	•	•	P	P								P	P	P		P	P				•	
New wafer production location or transfer of wafer production to a different not previously released location/site/subcontractor	•	•	•		•					•		•				J	•	•	•			•	
Wafer diameter	•	•			P					•		•				•						•	

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Table 3a: Process Change Guideline for LEDs (continued)

Table 2 test number	5 ab	6 ab	7	8a	10 ab	12	13	15	16	18 ab	19	20	21	22	23	24	25	26	27	28			
Name of test / Type of change	HTOL	WHTOL	TC	PTC	HBM/CDM	PD	TS	VVF	MS	RSH	SD	PLT	DEW	H2S	FMG	TR	WBP	WBS	DS	LF	TSK	PA	Remarks
BARE DIE DELIVERIES																							
New / change of front side metallization	•	•	•	•	M,B							•	•	•	•	•	•	•			•		
New / change of backside metallization	•	•	•	•	D,M					•		•	•	•	•	•			•		•		Customer application needs to be checked due to potential system voltage differences
Change of wafer setup or number of dies on wafer.																							
New final wafer thickness	•	P	•	•	P	•				•		•				•	B	B	•			•	
Change in coating or passivation	•	•	•	P	P					•			P	P	P		P	P				•	
PROCESS - ASSEMBLY																							
Change of leadframe/carrier base material	P	•	•				3			•	•		A	A	A	P,1	•	•	•	P			Explanation to provide in case H2S test is not applicable
Change of leadframe/carrier finishing material (internal)	P	•	•	•						•	•		A	A	A	P,1	•	•	•				Considered H2S test for exterior applications. Explanation to provide in case H2S test is not applicable
Change of lead and heat slug plating material/plating thickness (external)	P	K	•			1				•	•		A	A	A	P,1				K			Explanation to provide in case H2S test is not applicable
Bump Material / Metall System (internal)	•	•	•	•						•			W	W	W	•			•		•		
Die attach material	•	•	•	•				N	N	•			N	Q	Q	•			•		N		
Change of bond wire material	•	P,D	•	•				D	D	•		•		P,D	P,D		•	•			D		Site audit for material change with impact on bond process (e.g. from Au to Cu) recommended.
Change in material for sub-components (excluding LED chip & LED package related items) with impact on agreed specifications	Qualification effort depends on type of change.																						
Die Overcoat / Underfill	•	P	•	•	-	-		-	P	•	-	•	-	P	P	U			U		P		
Change of mold compound/encapsulation/sealing material	•	•	-	•	-	D	3	D	D	•	T	P	P	P	P	P					P		
Change of conversion material	•	•	Y	•				Y	Y	•		P	P	P	P	Y					Y	•	
Change of direct supplier for converter material	•	•	P	•				P	P	•		P	P	P	P	P					P	•	
Change of converter process technology	•	•	Y	•				Y	Y	•		Z	Z	Z	Z	Y					Y	•	
Change of product marking			O							T	T												
Change in process technique (e.g. die attach, molding, plating, trim & form,..)	Qualification effort depends on type of change.																						
Process Integrity: Tuning within specification																							
Change of direct material supplier with no impact on specification																							See change of material.
Change of specified-assembly process sequence (additional or deletion of process step)	Qualification effort depends on type of change.																						
New assembly location or transfer of assembly to a different not previously released location/site/subcontractor	Qualification effort depends on type of change.																						
PACKING/SHIPPING																							
Inner Packing/shipping specification change					P						T												
Outer Packing/shipping specification change																							
Change of labelling																							
Dry pack requirement change																							

Table 3a: Process Change Guideline for LEDs (continued)

Table 2 test number	5 ab	6 ab	7	8a	10 ab	12	13	15	16	18 ab	19	20	21	22	23	24	25	26	27	28			
Name of test / Type of change	HTOL	WHTOL	TC	PTC	HBM/CDM	PD	TS	VVF	MS	RSH	SD	PLT	DEW	H2S	FMG	TR	WBP	WBS	DS	LF	TSK	PA	Remarks
EQUIPMENT																							
Production from a new equipment/tool which uses a different basic technology	Qualification effort depends on type of change.																						
Production from a new equipment/tool which uses the same basic technology (replacement equipment or extension of existing equipment pool) without change of process.	Qualification effort depends on type of change.																						
Change in final test equipment type that uses a different technology					•						T											•	Gage R&R / delta correlation
TEST FLOW																							
Move of all or part of electrical wafer test and/or final test to a different not previously released location/site/subcontractor	B	•	•	B	•					•	T	B					B	B	B		B	•	Gage R&R / delta correlation; addtional specification check
Q-GATE																							
Change of the test coverage/testing process flow used by the supplier to ensure data sheet compliance (e.g. elimination/addition of electrical measurement/test flow block; relaxation/enhancement of monitoring procedure or sampling)																						•	

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Table 3b: Process Change Guideline for Lasers

Table 2 test number	5 ab	6 ab	7	8a	9	10 ab	12	13	14	14	16	17	18 ab	19	20	21	22	23	24	25	26	27	28			
Name of test	High Temperature Operating Life	Wet High temperatur Operating Life	Temperature Cycling	Power Temperature Cycling	Low Temperature Operating Life	ESD Characterization	Physical Dimensions	Terminal Strenght	Constant Acceleration	Vibration Variable Frequency	Mechanical Shock	Hermeticity	Resist. to Solder Heat	Solderability	Pulse Life Test	Dew Test	Hydrogen Sulphide	Flow Mixed Gas Corosion	Thermal Resistance	Wire Bond Strength	Wire Bond Shear	Die Shear	Leadfree	Thermal Shock	Parameter-Analysis: Comparison of current with	
Type of change	HTOL	WHTOL	TC	PTC	LTOL	HBM/CDM	PD	TS	CA	VVF	MS	HER	RSH	SD	PLT	Dew	H2S	FMGC	TR	WBS	BS	DS	LF	TSk	PA	Remarks
ANY																										
Any change with impact on agreed upon contractual agreements																										
Any change with impact on technical interface or processability/manufacturabiliy of customer			T										S,T													
DATA SHEET																										
Change of datasheet parameters/electrical specification (min./max./typ. values) and/or Pulse/DC specification	E	E	E		E	E							S		E				E						E	
Correction of data sheet																										
Specification of additional parameters																										• Formalism since this is not a product change, any addtional information.
DESIGN																										
Design changes in epitaxy.	•	•		•		•									•	H			•						•	
Design changes in routing/layout.	•	•	•	•									•		•	M	M	M		B	B	D,M		B, D,M	•	TR might be considered for complex die bond technologies
Die shrink	•	•	•	•	•	•							•		•				•	B	B	•			•	
Laser package (except leadframe, but including internal components)	•	•	•	•	•		•	3	•	•	•	4	•	T		D	D	D	L	B	B	D		•	•	
Design of leadframe	•	•	•	•		•	•	3	•	•	•	4	•	T					•	B	B	D	2	•	•	
PROCESS - WAFER PRODUCTION																										
New / change of wafer substrate or carrier material	•	P, V	P	•		P							•		•	P, V	P	P	•			•		P	•	
Wafer diameter	•	V				P							•		•				•						•	
New final wafer thickness	•	P, V	•	•		P									•				•	B	B	•			•	
Change of electrically active doping/implantation element	•	C, V		C		•									•				•						•	
Change of stacking	•	V	F	•		•									•	F, V									•	
New / change of metallization (specifically chip frontside)	•	V	•	•		M,B									•	M, V	M	M		•	•			B	•	
New / change of metallization (specifically chip backside)	•	V	•	•		D,M							•		•	D,M,V	D,M	D,M	D,M			•		D,M	•	
Change in process technique (e.g. significant process changes like lithography, etch, oxide deposition, die back surface preparation/backgrind, ...)	Qualification effort depends on type of change.																									
Process Integrity: Tuning within specification																										
Change of material supplier with no impact on agreed specifications	Qualification effort depends on type of change.																									
Change of specified wafer process sequence (deletion and/or additional process step)	Qualification effort depends on type of change. PPAP has to be updated.																									
New / change of facet passivation	•	V	•	•	•	•							•		•	V	P,V	P,V								
Change in die coating or passivaton	•	V	•	P		P										P,V	P,V	P,V		P	P				•	
New wafer production location or transfer of wafer production to a different not previously released location/site/subcontractor	•	V	•			•							•		•				J	•	•	•			•	
Wafer diameter	•	V				P							•		•				•						•	

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Table 3b: Process Change Guideline for Lasers (continued)

Table 2 test number	5 ab	6 ab	7	8a	9	10 ab	12	13	14	14	16	17	18 ab	19	20	21	22	23	24	25	26	27	28			
Name of test / Type of change	HTOL	WHTOL	TC	PTC	LTOL	HBM/CDM	PD	TS	CA	VVF	MS	HER	RSH	SD	PLT	Dew	H2S	FMGC	TR	WBS	BS	DS	LF	TSk	PA	Remarks
PROCESS - ASSEMBLY																										
Change of leadframe/carrier base material	P	•	•	•				3					•	•		A	A	A	P,1	•	•	•	P			Explanation should be provided in case H2S test is not applicable
Change of leadframe/carrier finishing material (internal)	P	•	•	•									•	•		A	A	A	P,1	•	•	•				H2S test should be considered for automotive exterrior applications. explanation should be provided in case H2S test is not applicable
Change of lead and heat slug plating material/plating thickness (external)	P	K	•				1						•	•		A	A	A	P,1				K			Explanation should be provided in case H2S test is not applicable
Bump Material / Metall System (internal)	•	•	•	•									•			W	W	W	•			•		•		
Die attach material	•	•	•	•					N	N	N		•			N	Q	Q	•			•		N		
Change of bond wire material	•	P,D	•	•					D	D	D		•		•		P,D	P,D		•	•			D		Site audit for material change with impact on bond process (e.g. from Au to Cu) recommended.
Change in material for sub-components (excluding Laser chip & Laser package related items) with impact on agreed specifications	Qualification effort depends on type of change.																									
Die Overcoat / Underfill	•	P	•	•					P	P	P		•		•		P	P	U			U		P		
Change of mold compound/encapsulation/sealing material	•	•		•			D	3	D	D	D	4	•	T	P	P	P	P	P					P		
Change of conversion material	•	•	Y	•					Y	Y	Y		•		P	P	P	P	Y					Y	•	
Change of direct supplier for converter material	•	•	P	•					P	P	P		•		P	P	P	P	P					P	•	
Change of converter process technology	•	•	Y	•					Y	Y	Y		•		Z	Z	Z	Z	Y					Y	•	
Assembly of additional internal components (e.g. lenses)	Qualification effort depends on type of change.																									
Change of material and / or supplier of additional internal components (e.g. lenses)	Qualification effort depends on type of change.																									
Generation of hermeticity (e.g. welding, gluing of transmissive window)	4		4	4					4	4	4	4	4				4	4						4		
Change of product marking			O										T	T												
Change in process technique (e.g., die attach, bonding, moulding, plating, trim and form, …)	Qualification effort depends on type of change.																									
Process Integrity: Tuning within specification																										
Change of direct material supplier with no impact on specification																										See change of material.
Change of specified-assembly process sequence (additional or deletion of process step)	Qualification effort depends on type of change.																									
New assembly location or transfer of assembly to a different not previously released location/site/subcontractor	Qualification effort depends on type of change.																									
PACKING/SHIPPING																										
Inner Packing/shipping specification change						P								T												
Outer Packing/shipping specification change																										
Change of labelling																										
Dry pack requirement change																										

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Table 3b: Process Change Guideline for Lasers (continued)

Table 2 test number	5 ab	6 ab	7	8a	9	10 ab	12	13	14	14	16	17	18 ab	19	20	21	22	23	24	25	26	27	28			
Name of test / Type of change	HTOL	WHTOL	TC	PTC	LTOL	HBM/CDM	PD	TS	CA	VVF	MS	HER	RSH	SD	PLT	Dew	H2S	FMGC	TR	WBS	BS	DS	LF	TSk	PA	Remarks
EQUIPMENT																										
Production from a new equipment/tool which uses a different basic technology	Qualification effort depends on type of change.																									
Production from a new equipment/tool which uses the same basic technology (replacement equipment or extension of existing equipment pool) without change of process.	Qualification effort depends on type of change.																									
Change in final test equipment type that uses a different technology						•								T											•	Gage R&R / delta correlation
TEST FLOW																										
Move of all or part of electrical wafer test and/or final test to a different not previously released location/site/subcontractor	B	•	•	B		•							•	T	B					B	B	B		B	•	Gage R&R / delta correlation; addtional specification check
Q-GATE																										
Change of the test coverage/testing process flow used by the supplier to ensure data sheet compliance (e.g. elimination/addition of electrical measurement/test flow block; relaxation/enhancement of monitoring procedure or sampling)																									•	

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Table 3c: Process Change Guideline for Photodiodes & Phototransistors

Table 2 test number	5c	6c	7	8b	10 ab	12	13	15	16	18	19	21	22	23	24	25	26	27	28			
Name of test / Type of change	High Temperature Reverse Bias	High Humidity High Temperature Reverse Bias	Temperature Cycling	Intermittend Operating Life	ESD Characterization	Physical Dimensions	Terminal Strenght	Vibration Variable Frequency	Mechanical Shock	Resist. to Solder Heat	Solderability	Dew Test	Hydrogen Sulphide	Flow Mixed Gas Corosion	Thermal resistance	Wire Bond Strength	Wire Bond Shear	Die Shear	Leadfree	Thermal Shock (for Robustness Validation only)	Parameter-Analysis: Comparison of current with changed device	
	HTRB	H³TRB	TC	IOL	HBM/CDM	PD	TS	VVF	MS	RSH	SD	Dew	H2S	FMGC	TR	WBS	BS	DS	LF	TSK	PA	Remarks
ANY																						
Any change with impact on agreed upon contractual agreements																						
Any change with impact on technical interface or processability/manufacturabiliy of customer			T							S,T												
DATA SHEET																						
Change of datasheet parameters/electrical specification (min./max./typ. values) and/or Pulse/DC specification	E	E	E		E					S					E						E	
Correction of data sheet																						
Specification of additional parameters																					•	Formalism since this is not a product change, any addtional information.
DESIGN																						
Design changes in epitaxy.	•	•		•	•							H									•	
Design changes in routing/layout.	•	•	•	•						•		M	M	M		B	B	D,M		B, D,M	•	TR might be considered for complex die bond technologies
Die shrink	•	•	•	•	•					•					•	B	B	•			•	
Component package (except leadframe)	•	•	•	•		•	3	V	V	•	T	D	D	D	L	B	B	D			•	
Design of leadframe	•	•	•	•	•	•	3	V	V	•	T				•	B	B	D	2	•	•	
PROCESS - WAFER PRODUCTION																						
New / change of wafer substrate or carrier material	•	P	P	•	P					•		P	P	P	•			•		P	•	
Wafer diameter	•	•			P					•					•						•	
New final wafer thickness	•	P	•	•	P										•	B	B	•			•	
Change of electrically active doping/implantation element	•	C		C	•										•						•	
Change of stacking	•	•	F	•	•							F									•	
New / change of metallization (specifically chip frontside)	•	•	•	•	M,B							M	M	M		•	•			B	•	
New / change of metallization (specifically chip backside)	•	•	•	•	D,M					•		D,M	D,M	D,M	D,M			•		D,M	•	
Change in process technique (e.g. significant process changes like lithography, etch, oxide deposition, die back surface preparation/backgrind, ...)	Qualification effort depends on type of change.																					
Process Integrity: Tuning within specification																						
Change of material supplier with no impact on agreed specifications	Qualification effort depends on type of change.																					
Change of specified wafer process sequence (deletion and/or add. process step)	Qualification effort depends on type of change. PPAP has to be updated.																					

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Table 3c: Process Change Guideline for Photodiodes & Phototransistors (continued)

Table 2 test number	5c	6c	7	8b	10 ab	12	13	15	16	18	19	21	22	23	24	25	26	27	28			
Name of test / Type of change	HTRB	H³TRB	TC	IOL	HBM/CDM	PD	TS	VVF	MS	RSH	SD	Dew	H2S	FMGC	TR	WBS	BS	DS	LF	TSK	PA	Remarks
PROCESS - WAFER PRODUCTION - continued																						
Change in die coating or passivaton	•	•	•	P	P							P	P	P		P	P				•	
New wafer production location or transfer of wafer production to a different not previously released location/site/subcontractor	•	•	•		•					•					J	•	•	•			•	
Wafer diameter	•	•			P					•					•						•	
BARE DIE DELIVERIES																						
New / change of front side metallization	•	•	•	•	M,B							•	•	•	•	•	•			•		
New / change of backside metallization	•	•	•	•	D,M					•		•	•	•	•			•		•		customer application needs to be checked due to potential system voltage differences
Change of wafer setup or number of dies on wafer.																						
New final wafer thickness	•	P	•	•	P	•				•					•	B	B	•			•	
Change in coating or passivation	•	•	•	P	P					•		P	P	P		P	P				•	
PROCESS - ASSEMBLY																						
Change of leadframe/carrier base material	P	•	•				3			•	•	A	A	A	P,1	•	•	•	P			Explanation to provide in case H2S test is not applicable
Change of leadframe/carrier finishing material (internal)	P	•	•	•						•	•	A	A	A	P,1	•	•	•				Consider H2S test for exterior applications. Explanation to provide in case H2S test is not applicable
Change of lead and heat slug plating material/plating thickness (external)	P	K	•			1				•	•	A	A	A	P,1				K			Explanation to provide in case H2S test is not applicable
Bump Material / Metall System (internal)	•	•	•	•						•		W	W	W	•			•		•		
Die attach material	•	•	•	•				N	N	•		N	Q	Q	•			•		N		
Change of bond wire material	•	P,D	•	•				D	D	•			P,D	P,D		•	•			D		Site audit for material change with impact on bond process (e.g. from Au to Cu) recommended.
Change in material for sub-components (excluding photodiode/transistor chip & package related items) with impact on agreed specifications	Qualification effort depends on type of change.																					
Die Overcoat / Underfill	•	P	•	•					P	•			P	P	U			U		P		
Change of mold compound/encapsulation/sealing material	•	•	•	•		D	3	D	D	•	T	P	P	P	P					P		
Change of product marking			O							T	T											
Change in process technique (e.g. die attach, molding, plating, trim & form,..)	Qualification effort depends on type of change.																					
Process Integrity: Tuning within specification																						
Change of direct material supplier with no impact on specification																						See change of material.
Change of specified assembly process sequence (additional or deletion of process step)	Qualification effort depends on type of change.																					
New assembly location or transfer of assembly to a different not previously released location/site/subcontractor	Qualification effort depends on type of change.																					

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Table 3c: Process Change Guideline for Photodiodes & Phototransistors (continued)

Table 2 test number	5c	6c	7	8b	10 ab	12	13	15	16	18	19	21	22	23	24	25	26	27	28			
Name of test / Type of change	HTRB	H³TRB	TC	IOL	HBM/CDM	PD	TS	VVF	MS	RSH	SD	Dew	H2S	FMGC	TR	WBS	BS	DS	LF	TSK	PA	Remarks
PACKING/SHIPPING																						
Inner Packing/shipping specification change					P						T											
Outer Packing/shipping specification change																						
Change of labelling																						
Dry pack requirement change																						
EQUIPMENT																						
Production from a new equipment/tool which uses a different basic technology	Qualification effort depends on type of change.																					
Production from a new equipment/tool which uses the same basic technology (replacement equipment or extension of existing equipment pool) without change of process.	Qualification effort depends on type of change.																					
Change in final test equipment type that uses a different technology					•						T										•	Gage R&R / delta correlation
TEST FLOW																						
Move of all or part of electrical wafer test and/or final test to a different not previously released location/site/subcontractor	B	•	•	B	•					•	T					B	B	B		B	•	Gage R&R / delta correlation; addtional specification check
Q-GATE																						
Change of the test coverage/testing process flow used by the supplier to ensure data sheet compliance (e.g. elimination/addition of electrical measurement/test flow block; relaxation/enhancement of monitoring procedure or sampling)																					•	

Appendix 1: Definition of a Qualification Family

The qualification of a particular process will be defined within, but not limited to, the categories listed below. The supplier will provide a complete description of each process and material of significance. Valid evidence for the link between the data and the subject of qualification has to be provided by the supplier.

For parts to be categorized in a qualification family, they all must share the same major process and materials elements as defined below. For each qualification test, two or more qualification families can be combined if the reasoning is technically sound (i.e., supported by rationale clearly detailing similarity). All parts using the same process and materials are to be categorized in the same qualification family for that process and are acceptable by association when one family member successfully completes qualification with the exception of the device specific requirements of Section 4.2.

Prior qualification data 3 years old or newer obtained from a part in a specific family may be extended to the qualification of subsequent parts in that family provided the supplier can insure no process changes have been made.

For broad changes that involve multiple attributes (e.g., site, material(s), process(es)), refer to Section 2.2 that allows for the selection of worst-case test vehicles to cover all the possible permutations.

A1.1 Fab Process

Each process technology (e.g., LED, Photo Diodes, etc.) must be considered and subjected to stress-test qualification separately. No matter how similar, processes from one fundamental fab technology cannot be used for the other.

Family requalification with the appropriate tests is required when the process or a material is changed. The important attributes defining a qualification family are listed below:

A1.1.1 Wafer Fab Technology

- LEDs
- Phototransistors
- Photo Diodes
- Laser Diodes

A1.1.2 Wafer Fab Process - consisting of the same attributes listed below:

- Process flow
- Layout design rules
- Number of masks
- Basic epitaxial process (e.g., InGaN vs. InGaAlP)
- Lithographic process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)
- Etching process (e.g., dry vs. wet etching)
- Doping process (e.g., diffusion vs. ion implantation)
- Passivation/Coating material and thickness range
- Oxidation and deposition process and thickness range
- Front/back metallization material and thickness range
- Wafer bonding and lift off process

A1.1.3 Wafer Fab Site

A1.2 Assembly Process

The processes for each package type must be considered and subjected to stress-test qualification separately. For parts to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification with the appropriate tests is required when the process or a material is changed. The supplier must submit technical justification to the user(s) to support the acceptance of generic data with package and die type, different than the device being considered for stress-test qualification. The important attributes defining a qualification family are listed below:

A1.2.1 Package Type

Examples include Radial, PLCC-x, Chip on Board, Chip Scale Package, etc.

A1.2.2 Assembly Process - consisting of the same attributes listed below:

- Leadframe base material
- Leadframe plating (internal and external to the package)
- Die attach material/method
- Wire bond material, wire diameter, and process
- Plastic mold compound or other encapsulation material
- Converter material/method

A1.2.3 Assembly Site

A1.2.4 Example

3 lots of a package family using any die structure that has the same die backside metallization will suffice for the following Qualification tests. It is highly desirable that two of the lots come from the maximum and minimum die size allowed by the package design rules.

- HTOL
- TC
- PTC
- WHTOL

A1.3 Qualification of Multiple Families and Sites

When the specific product or process attribute to be qualified or re-qualified (i.e., via process, material or site change) will affect more than one wafer fab family or assembly family, the qualification test vehicles should be three lots of a single part type from each of the technology and package families that are projected to be most sensitive to the changed attribute with sample sizes split to include a minimum of 26 pieces from each of 3 assembly lots from each assembly / fab site.

Below is the recommended process for qualifying changes across many process and product families:

a. Identify all products affected by the proposed process changes.

b. Identify the critical structures and interfaces potentially affected by the proposed change.

c. Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces. Conduct a risk assessment into potential failure mechanisms. Note that steps (a) to (c) are equivalent to the creation of an FMEA.

d. Define the product groupings or families based upon similar characteristics as they relate to the technology process and package families and device sensitivities to be evaluated, and provide technical justification to document the rationale for these groupings.

e. Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products, which will address each of the potential failure mechanisms and associated failure modes.

f. Robust process capability must be demonstrated at each site (e.g., control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process step(s).

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Appendix 2: AEC-Q102 Certification of Design, Construction and Qualification

Supplier Name: **Date:**

The following information is required to identify a part that has met the requirements of AEC-Q102. Submission of the required data in the format shown below is optional. **All entries must be completed; if a particular item does not apply, enter "Not Applicable".** This template can be downloaded from the AEC website at http://www.aecouncil.com.

Item Name	Supplier Response
1. User's Part Number:	
2. Supplier Part Number/Generic Part Number:	
3. Device Description:	
4. Wafer/Die Fab Location & Process ID: a. Facility name/plant #: b. Street address: c. Country:	
5. Wafer Probe Location: a. Facility name/plant #: b. Street address: c. Country:	
6. Assembly Location & Process ID: a. Facility name/plant #: b. Street address: c. Country:	
7. Final Quality Control (Test) Location: a. Facility name/plant #: b. Street address: c. Country:	
8. ESD-protective device a. Manufacturer: b. Facility name/plant #:	
9. Wafer/Die: a. Wafer size: b. Die family: c. Die mask set revision & name:	
10. Wafer/Die Technology Description: a. Wafer/Die process technology: b. Substrate material c. Number of mask steps:	
11. Die Dimensions: a. Die width: b. Die length: c. Die thickness (finished):	
12. Die (frontside) Metallization: a. Die metallization material(s): b. Number of layers: c. Thickness (per layer): d. % of alloys (if present):	
13. Die Passivation: a. Number of passivation layers: b. Die passivation material(s): c. Thickness(es) & tolerances:	

14. Die Overcoat Material	
15. Die Prep Backside: a. Die prep method: b. Die metallization: c. Thickness(es) & tolerances:	
16. Die Separation Method: a. Kerf width (µm): b. Kerf depth (if not 100% saw): c. Saw method:	Single ☐ Dual ☐
17. Die Attach: a. Die attach material ID: b. Die attach method: c. Die placement diagram:	See attached ☐ Not available ☐
17. Package: a. Type of package (e.g., plastic, ceramic, unpackaged): b. JEDEC designation (e.g. PLCC etc.):	
18. Mold Compound a. Mold compound supplier & ID: b. Mold compound type: c. Flammability rating: d. Fire Retardant type/composition: e. Tg (glass transition temperature)(°C): f. CTE (above & below Tg)(ppm/°C):	UL 94 V1 ☐ UL 94 V0 ☐ CTE1 (below Tg) = _____ CTE2 (above Tg) = _____
19 Encapsulation/Casting material: a. Encapsulation material supplier & ID: b. Encapsulation material type: c. Tg (glass transition temperature)(°C): d. CTE (above & below Tg)(ppm/°C):	
20. Wire Bond: a. Wire bond material: b. Wire bond diameter (mils): c. Type of wire bond at die: d. Type of wire bond at leadframe: e. Number of bonds over active area:	
21. Leadframe: a. Leadframe material: b. Leadframe bonding plating composition: c. Leadframe bonding plating thickness (µinch): d. External lead plating composition: e. External lead plating thickness (µinch): f.. External lead plating technology:	
22. Board Material: a. Board material supplier & ID: b. Board material type: c. CTE:	
23. Converter: a. Converter material supplier & ID: b. Converter material type:	

24. Thermal Resistance: a. $\theta_{Junction - Ambient}$ °C/W (approx): b. $\theta_{Junction - SolderJoint}$ °C/W (approx): c.	
25. Maximum Process Exposure Conditions: a. MSL @ rated SnPb temperature: b. MSL @ rated Pb-free temperature: J-STD-020x fulfilled:	* Note: Temperatures are as measured on the center of the plastic package body top surface. at °C (SnPb) at °C (Pb-free) ☐ yes - revision: ☐ no

Attachments:		Requirements:
Die Photo	☐	1. A separate Certification of Design, Construction & Qualification must be submitted for each part number, wafer fab, and assembly location.
Package Outline Drawing	☐	
Die Cross-Section Photo/Drawing	☐	
Wire Bonding Diagram	☐	2. Design, Construction & Qualification shall be signed by the responsible individual at the supplier who can verify the above information is accurate and complete. Type name and sign below.
Die Placement Diagram	☐	

Completed by: Date:	Certified by: Date:
Typed or Printed: Signature: Title:	

This template is available as a stand-alone document that can be downloaded at http://www.aecouncil.com.

Appendix 3: AEC-Q102 Qualification Test Plan

The supplier is requested to complete and submit the Discrete Optoelectronic Semiconductor Qualification Test Plan as part of the pre-launch Control Plan whenever qualification submission is required. Acceptance and subsequent sign-off of the plan will establish a qualification agreement between the user and the supplier determining requirements for both new parts and process changes prior to commencement of testing. Where "family" data is being proposed, the plan will document how the reliability testing previously completed fulfills the requirements outlined in this specification. An approved copy of the Qualification Test Plan shall be included with each qualification submission.

The test plan section of the form should detail ONLY the testing that will be performed on the specific part shown. For process change qualifications, multiple parts can be included on the same plan. Supporting generic or family data reports should be noted in the comment section and attached. When requesting use of generic or family data, attach a separate page detailing similarities or differences between parts referencing the criteria in Appendix 1. There must be valid and obvious links between the data and the subject of qualification.

The example below is provided to demonstrate how the Qualification Test Plan Form, found on the AEC website, should be used. In this case, a discrete part was chosen as being representative of a typical new part qualification requesting reduced component testing by including generic test data. The part comes from a supplier who previously qualified the package, assembly site, etc. This example is shown for illustration purposes only and should not limit any requirements from Table 1 herein.

Rev. A	Discrete Optoelectronic Semiconductor Qualification Plan		
User P/N:	*5317704*	User Component Engineer:	*A. Young*
User Spec. #:	*5317704-XX*	General Specification:	*AEC-Q102*
Supplier:	*Bruno's Best LED*	Supplier Manufacturing Site:	*Sydney, Australia*
Supplier Generic P/N:	*EVE*	Required PPAP Subimission Date:	*14. Nov 16*
Supplier Internal P/N:	*EVE-2001*	Family Type:	*CSP 3 W*
Reason for Qual.:	*New device qualification*		

Item	Test	Test Conditions	Remarks / Exceptions	Est. Start	Est. End	# Lots	S.S. per lot
1	*TEST*	*per AEC Q-102 rev. A*		*1. Apr 16*	*5. Apr 16*	*all*	*all*
2	*PC*	*per AEC Q-102 rev. A; MSL 2a*		*6. Apr 16*	*8. Apr 16*	*all*	*all*
3	*EV*	*per AEC Q-102 rev. A*		*9. Apr 16*	*10. Apr 16*	*all*	*all*
4	*PV*	*per AEC Q-102 rev. A*		*11. Apr 16*	*16. Apr 16*	*3*	*26*
5	*HTOL1*	*per AEC Q-102 rev. A*	*Use attached generic data*	*20. Apr 16*	*8. Jun 16*	*3*	*26*
6	*HTOL2*	*per AEC Q-102 rev. A; Ts=80°; If=1500mA, Tj = 150°*		*20. Apr 16*	*8. Jun 16*	*3*	*26*
7	*WHTOL1*	*per AEC Q-102 rev. A*	*Use attached generic data*	*20. Apr 16*	*8. Jun 16*	*3*	*26*
8	*WHTOL2*	*per AEC Q-102 rev. A; If= 50mA, delta Tj = 2K*		*20. Apr 16*	*8. Jun 16*	*3*	*26*
9	*TC*	*per AEC Q-102 rev. A; condition 4*		*20. Apr 16*	*8. Jun 16*	*3*	*26*
...	*...*	*...*		*...*	*...*	*...*	*...*

Failure criteria
(according to AEC-Q102 Appendix 5 if not specified else)

Parameter	Acceptance Criteria	Remark
Luminous flux	*+/- 20% from initial value*	*If = 1000mA; T= 25°*
Colour coordinates	*+/- 0,01 from initial value*	*If = 1000mA; T= 25°*
Forward Voltage	*+/- 10% from initial value*	*If = 1000mA; T= 25°*
Forward Voltage	*+/- 10% from initial value*	*If = 50mA; T= 25°*
Forward Voltage	*light / no light*	*T = -40° & 120°*
Visual	*migration, corrosion, delamination, other*	

Comments:
1. *These devices all share same the same wafer and assembly processes*
2. *Failure criteria for intensity is +/- 30%*
3. *Attached quarterly reliability results for 2014 & 2015 on EVE2001*

Prepared by (supplier)		Approved by (user)	
Typed/Printed		Typed/Printed	
Signature		Signature	
Title		Title	

* Note: This plan is only an example and does not represent all the required tests in this document.

Figure A3.1: Example of AEC-Q102 Qualification Test Plan

This template is available as a stand-alone document that can be downloaded at http://www.aecouncil.com.

Appendix 4: Data Presentation Format

The supplier is required to complete and submit an Environmental Test Summary and Parametric Verification Summary with each Discrete Optoelectronic Semiconductor PPAP submittal. Figure A4.1 is an example of a completed Environmental Test Summary.

In addition, the supplier has to provide test data for each individual part if requested by the user. The individual test data should be provided in graphic format (individual data points). Other formats may be chosen if agreed mutually by user and supplier.

Figure A4.2 is an example of a completed Parametric Verification Summary. The format of both summaries shall be followed.

Soft copies of the formats may be found on the AEC website or is available upon request. Other equivalent formats are acceptable if approved by the user.

Supplier	User Part Number	Reason for Qualification
Bruno's Best LED	*5317704*	*New device*
Name of Laboratory	**Part Description**	**Report #**
Bruno's Best LED Qual Lab	*EVE2001 (CSP 3W)*	*BBL-2016-04-01*
Production Site	**Lot #**	**Date**
Sydney, Australia	*BBL160001, BBL160002, BBL160003*	*01.04.2016*

Test #	AEC-Q102 Reference	Test Description	Test Conditions	# Lots	# Tested (each lot)	# Failed
2	*2*	*PC*	*per AEC Q-102 rev. A; MSL 2a*	*3*	*26*	*0*
3	*3*	*EV*	*per AEC Q-102 rev. A*	*3*	*494*	*0*
4	*4*	*PV*	*per AEC Q-102 rev. A*	*3*	*26*	*0*
5	*5a*	*HTOL1*	*per AEC Q-102 rev. A; Ts=120°; If=500mA, Tj = 150°*	*3*	*26*	*0*
6	*5b*	*HTOL2*	*per AEC Q-102 rev. A; Ts=80°; If=1500mA, Tj = 150°*	*3*	*26*	*0*
7	*6a*	*WHTOL1*	*per AEC Q-102 rev. A, If=1400mA; Tj=150°*	*3*	*26*	*0*
8	*6b*	*WHTOL2*	*per AEC Q-102 rev. A; If= 50mA, delta Tj = 2K*	*3*	*26*	*0*
9	*7*	*TC*	*per AEC Q-102 rev. A; condition 4*	*3*	*26*	*0*
10	*-*	*LTSL*	*Internal spe; 1000h; -40°; no bias*	*3*	*26*	*0*

Failure criteria
(according to AEC-Q102 Appendix 5 if not specified else)

Parameter	Acceptance Criteria	Remark
Luminous flux	*+/- 20% from initial value*	*If = 1000mA; T= 25°*
Colour coordinates Cx and Cy	*+/- 0,01 from initial value*	*If = 1000mA; T= 25°*
Forward voltage	*+/- 10% from initial value*	*If = 1000mA; T= 25°*
Forward voltage	*+/- 10% from initial value*	*If = 50mA; T= 25°*
Forward voltage	*light / no light*	*T = -40° & 120°*
Visual	*migration, corrosion, delamination, other*	

Name	*Bruno*
Department	*Quality*
Signature	*(signed)*

* Note: This listing of test results is only an example and does not represent all the tests in this document.

Figure A4.1: Environmental Test Summary Example

This template is available as a stand-alone document that can be downloaded at http://www.aecouncil.com.

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Supplier				**User Part Number**				
Bruno's Best LED				*5317704*				
Lot Number				**Temperature**				
BBL160001 (Test lot #1)				*25°C*				
Test Name	Unit	Spec LSL	Spec USL	Min	MAX	MEAN	STD DEV	Cpk
Iv	mcd	1440	4000	2264	2486	2522	50,4	6,51
Vf	V		3,8	3,3	3,3	3,3	0,02	15,2

Figure A4.2: Parametric Verification Summary Example

Appendix 5: Minimum Parametric Test Requirements and Failure Criteria

For Table 2 Test #1 (Pre- & Post-Stress Electrical Test), the following electrical and optical parameters shall be used (as a minimum):

LEDs:

Parameter	Acceptance criteria	Remark
Parameter to measure at room temperature		
Luminous flux or Intensity or Radiant power (whatever is appropriate)	+/- 20% Note. +/- 30% may be acceptable for some application. +/- 50% may be acceptable only for some application (e.g., interior). Choice of range to be noticed in the test report.	To measure at nominal rated current.
Color coordinates Cx & Cy or Dominant wavelength (for direct colors)	+/- 0.01 according to initial value Note: +/- 0.02 may be acceptable for H2S & FMG for some application (e.g., interior). Choice of range to be noticed in the test report. or +/- 2 nm according to initial value (for dominant wavelength)	
Forward voltage Vf	+/- 10%	
Forward voltage V_{min}	+/- 10%	To measure at minimum and maximum rated current. If no minimum drive current is specified, 10% of the nominal current should be chosen.
Parameter to measure at minimum & maximum temperature		
Forward voltage Vf	light / no light	To measure at nominal rated current. Consider derating.

Laser Components:

Parameter	Acceptance criteria	Remark
Parameter to measure at room temperature		
Luminous flux or Intensity or radiant power (whatever is appropriate)	+/- 20% Note: +/- 30% or +/- 50% may be acceptable for some application. Choice of range to be noticed in the test report.	To measure at nominal rated current.
Color coordinates Cx & Cy or Dominant wavelength (for direct colors)	+/- 0.02 according to initial value or +/- 2 nm according to initial value	
Forward voltage Vf	+/- 10%	
Forward voltage V_{min}	+/- 10%	To measure at minimum and maximum rated current. If no minimum drive current is specified, 10% of the nominal current should be chosen.
Peak luminance (max. luminance over whole light emitting area) or Average luminance	Same variation as chosen for luminous flux (intensity, radiant power respectively).	**For laser components with remote color conversion only. Applies only to HTOL, TC, PTC, VVF, MS, H2S, FMG.** Parameter to be measured at nominal rated current on 3 samples before/after. Choice of measuring area (size and position) to be noticed in the test report.
Radiation characteristic (intensity over angle)	n.a.	**For direct color laser only. Applies only to HTOL, TC, PTC, WHTOL.** The radiation characteristic has to be measured before and after the stress test. Data must be provided if requested by the customer.
Degree of polarization	n.a.	**For direct color laser only. Applies only to HTOL, TC, PTC, WHTOL.** The degree of polarization has to be measured before and after the stress test. Data must be provided if requested by the customer.
Parameter to measure at minimum & maximum temperature		
Forward voltage Vf	Vf-check for “open” (“light on/off test”)	To measure at nominal rated current. Consider derating.
Laser safety has to be maintained before and after test.		

Photodiodes:

Parameter	Acceptance criteria	Remark
Parameter to measure at room temperature		
Photo current	+/- 25%	
Dark current	+ 100%	No light exposure.
Forward voltage	+/- 10%	No light exposure.
Parameter to measure at minimum & maximum temperature		
Forward voltage	open / short	

Phototransistors:

Parameter	Acceptance criteria	Remark
Parameter to measure at room temperature		
Collector Light Current I_{CA}	+/- 25%	No light exposure.
Collector Emitter Breakdown Voltage $V_{(BR)CE0}$	+/- 20%	No light exposure. Functional limit: 95% from min. value specified in component datasheet.
Parameter to measure at minimum & maximum temperature		
V_{CE} & V_{BE}	open / short	

Appendix 6: Destructive Physical Analysis (DPA)

A6.1 Description

The purpose of this examination is to determine the capability of a device's internal materials, design, and workmanship to withstand forces induced by various stresses induced during environmental testing.

A6.2 Equipment:

a. Optical microscope having magnification capability of up to 50X
b. De-capsulation equipment
c. Cross section equipment

A6.3 Procedure:

a. Parts selected for this test must have successfully completed environmental testing as defined in Table 2, respectively Table 3a-c (Process Change Guidelines for the Selection of Tests) of AEC-Q102.
b. The parts shall be opened or de-capsulated in order to expose the internal die/substrate and determine the extent of any mechanical or chemical damage. The process used to de-capsulate the device must insure that it does not cause degradation of the leads and bonds. The internal die or substrate must be completely exposed and free of packaging material.
c. The devices shall be examined under a magnification of up to 50X to the criteria listed in Section A6.4, herein.
d. A cross section shall be done to analyze critical die structures (e.g., metallization layers, die attach, etc.), wire bonding connection and further critical internal component structures.
e. Failed devices shall be analyzed to determine the cause of the failure. A Failure Analysis Report documenting this analysis shall be prepared on all failures. If the analysis shows that the failure was caused by the package opening process, the test shall be repeated on a second group of parts.
f. Risk evaluation shall be done for failed devices and reported to the customer. Generic data, additional reliability tests and/or common literature may be used.

A6.4 Failure Criteria:

Devices shall be considered failed if they exhibit any of the following:

a. Visible evidence of non-conforming to the devices' Certificate of Design, Construction and Qualification.
b. Visible evidence of corrosion, contamination, delamination or metallization voids.
c. Visible evidence of die/substrate cracks or defects (e.g., scratches, glassivation, etc.).
d. Visible evidence of wire, die, or termination bond defects.
e. Visible evidence of dendrite growth or electromigration.

Appendix 7: Guidance on Relationship of Robustness Validation to AEC-Q102

A7.1 SCOPE

Successful completion of the test requirements in Table 2 allows the claim to be made that the part is AEC Q102 qualified. Additional testing may be agreed between Component Manufactures and Tier 1 Component Users depending on more demanding application environments. To address these more stringent conditions, application based Mission Profiles may be used for a reliability capability assessment.

A mission profile is the collection of relevant environmental and functional loads that a component will be exposed to during its use lifetime.

A7.1.1 Purpose

This appendix provides information on an approach that can be used to assess the suitability of a component for a given application and its mission profile for unique requirements. The benefit of applying this approach is that, in the end, the reliability margin between the component (specification) space and the application (condition) space may be shown.

- Section A7.2 demonstrates the relation between AEC-Q102 stress conditions / durations and a typical example of a set of use life time and loading conditions.
- Section A7.3 describes the approach, supported by flow charts, which can be used for a reliability capability assessment starting from a mission profile description.

A7.1.2 References

- **SAE J1879/J1211/ZVEI** Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
- **JEDEC JEP122** Failure Mechanisms and Models for Semiconductor Devices

A7.2 BASE CONSIDERATIONS

A7.2.1 Use Lifetime and Mission Profile

The use lifetime assumptions drawn here are an example used for demonstration purpose only. Many typical mission profiles will differ in one or more characteristics from what is shown below.

- service lifetime in years
- engine on-time in hours
- engine off time { idle} in hours
- non-operating time in hours
- number of engine on-off cycles
- service mileage

The mission profile itself is generated by adding information on thermal, electrical, mechanical and any other forms of loading under use conditions to the above lifetime characteristics. Examples of these and how they relate to the test conditions in Table 2 are shown in Table A7.1.

A7.2.2 Relation to AEC-Q102 Stress Test Conditions and Durations

The basic calculations in Table A7.1 for each of the major stress tests demonstrate how one can derive suitable test conditions for lifetime characteristics based on reasonable assumptions for the loading. Caution should always be taken on use of excessive test conditions beyond those in Table 2, because they may induce unrealistic fail mechanisms and/ or acceleration.

A7.3 METHOD TO ASSESS A MISSION PROFILE

This section demonstrates how to perform a more detailed reliability capability assessment in cases where the application differs significantly from existing and proven situations:

- Application has a demanding loading profile
- Application has an extended service lifetime requirement
- Application has a more stringent failure rate target over lifetime

These considerations may result in extended test durations. In addition, there may be components manufactured in new technologies and/or containing new materials that are not yet qualified. In such cases, unknown failure mechanisms may occur with different times-to-failure which may require different test methods and/or conditions and/or durations.

For these cases, two flow charts are available to facilitate both Tier 1 and Component Manufacturing in a reliability capability assessment:

- Flow Chart 1 in Figure A7.1, describes the process at Component Manufacturer to assess whether a new component can be qualified by AEC-Q102.
- Flow Chart 2 in Figure A7.2, describes (1) the process at Tier 1 to assess whether a certain electronic component fulfills the requirements of the mission profile of a new Electronic Control Unit (ECU); and (2) the process at Component Manufacturer to assess whether an existing component qualified according to AEC-Q102 can be used in a new application.

For details on how to apply this method, please refer to SAE J1879, SAE J1211 and/or ZVEI Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications.

In summary, the flow charts result in the following three clear possible conclusions:

[A] AEC-Q102 test conditions do apply.
[B] Mission Profile specific test conditions may apply.
[C] Robustness Validation may be applied with detailed alignment between Tier1 and Component Manufacturer.

In addition, not shown in the flow charts, the expected end of life failure rate may be an important criterion. Regarding failure rates, the following points should be considered:

- No fails in 78 devices (26 devices from 3 lots) are applied as pass criteria for the major environmental stress tests. This represents an LTPD (Lot Tolerance Percent Defective) = 3, meaning a maximum of 3% failures at 90% confidence level.
- This sample size is sufficient to identify intrinsic design, construction and/or material issues affecting performance.
- This sample size is NOT sufficient or intended for process control or PPM evaluation. Manufacturing variation failures (low ppm issues) are achieved through proper process controls and/or screens such as described in AEC-Q001 and -Q002.
- Three lots are used as a minimal assurance of some process variation between lots. A monitoring process has to be installed to keep process variations under control.
- Sample sizes are limited by part and test facility costs, qualification test duration and limitations in batch size per test.

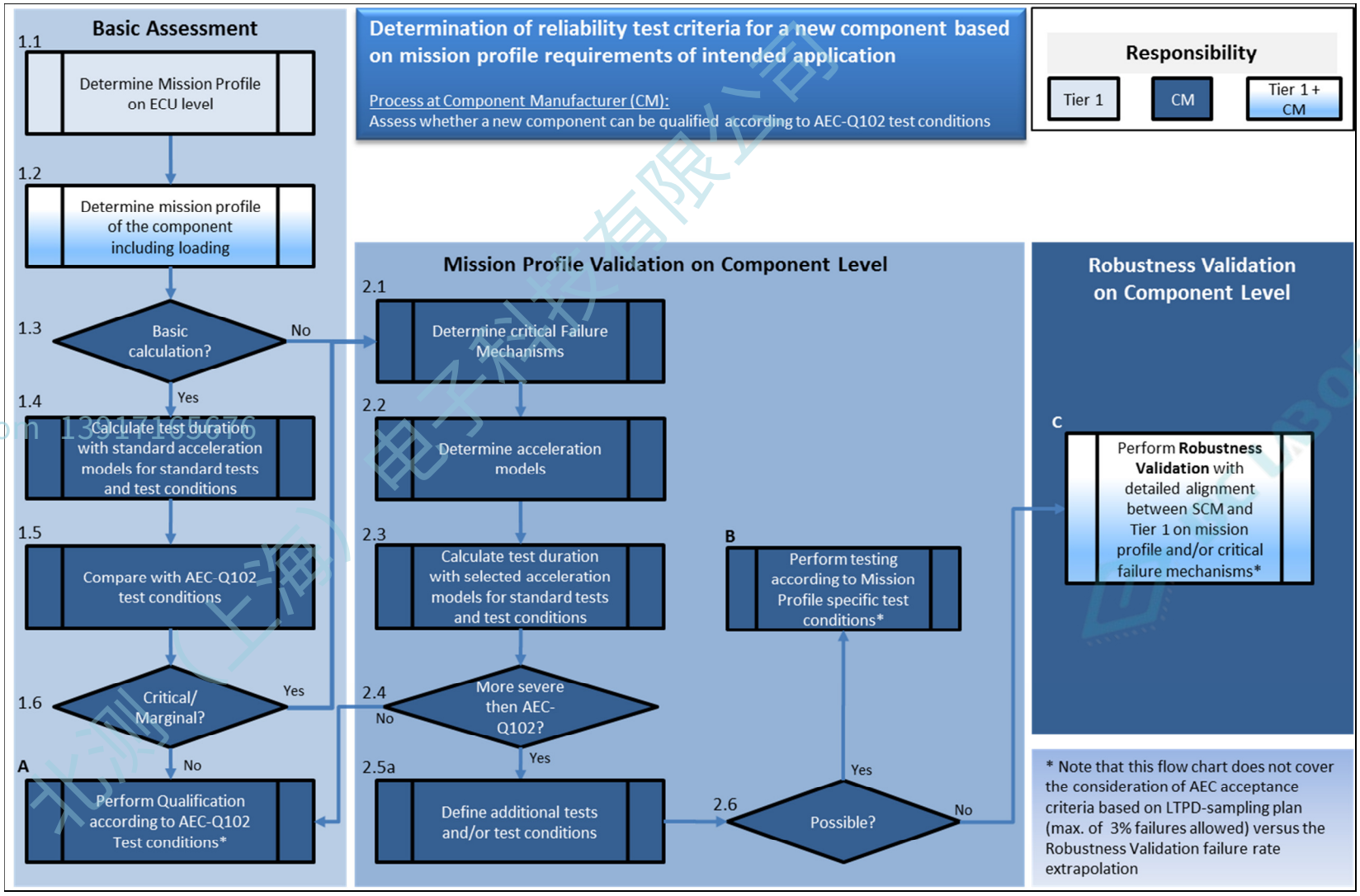

Figure A7.1: Flow Chart 1 – Reliability Test Criteria for New Component

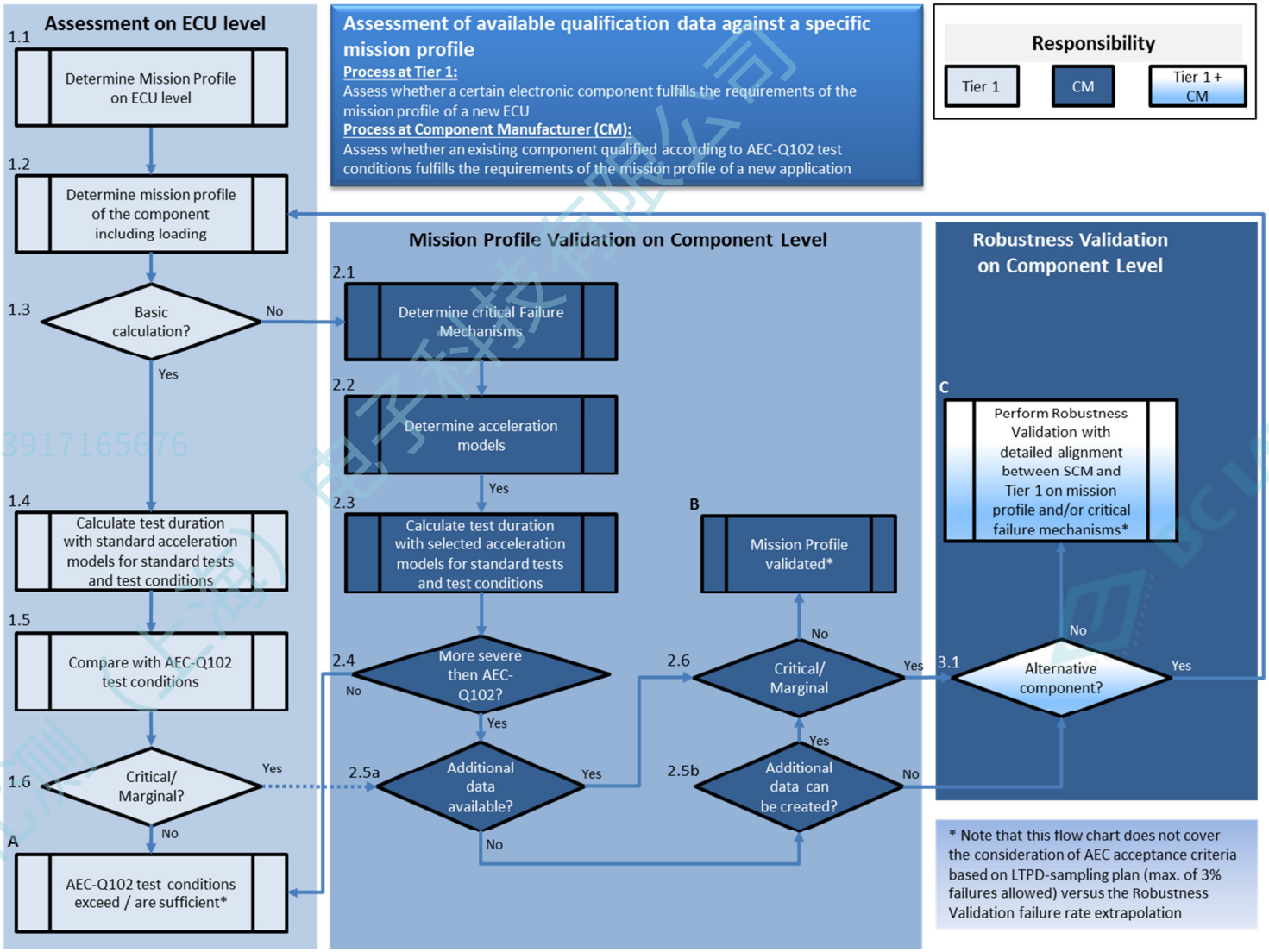

Figure A7.2: Flow Chart 2 – Assessment of Existing, Qualified Component

Table A7.1: Example Calculations for AEC-Q102 Tests for Discrete Devices

Loading	Mission Profile Input	Stress Test	Stress Conditions	Acceleration Model (all temperatures in K, not in ℃)	Model Parameters	Calculated Test Duration	Q102 Test Duration
Operation	t_u = 12,000 h (average operating use time over 15 years) T_u = 100 ℃ (average junction temperature in use environment)	High Temperature Operating Life (HTOL) or High Temperature Reverse Bias (HTRB)	T_t = 150 ℃ (junction temperature in test environment)	Arrhenius $A_f = \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$ Also applicable for High Temperature Storage Life (HTSL)	E_a = 0.7 eV (activation energy; 0.7 eV is a typical value, actual values depend on failure mechanism and range from -0.2 to 1.4 eV) k_B = 8.61733 x 10^{-5} eV/K (Boltzmann's Constant)	t_t = 916 h (test time) $t_t = \frac{t_u}{A_f}$	1000 h
Thermo-mechanical	n_u = 54,750 cycles (number of engine on/off cycles over 15 years of use) ΔT_u =70 K (average thermal cycle temperature change in use environment)	Temperature Cycling (TC)	ΔT_t =205 K (thermal cycle temperature change in test environment: -55 ℃ to 150 ℃)	Coffin Manson $A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$	m = 4 (Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials)	n_t =744 cycles (number of cycles in test) $n_t = \frac{n_u}{A_f}$	1000 cycles
	n_u = 54,750 cycles (number of engine on/off cycles over 15 years of use) ΔT_u =55 K for solder die attach (average thermal cycle temperature change in use environment)	Intermittent Operational Life (IOL)	ΔT_t =100℃ (thermal cycle temperature change in test environment: 25 ℃ to 125 ℃)	Coffin Manson $A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$ Also applicable for Power Temperature Cycle (PTC) Remark: The use of a Coffin-Manson model may not be appropriate to reflect time dependence of material behavior.	m = 2.5 (Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials)	n_t =12,283 cycles (number of cycles in test) $n_t = \frac{n_u}{A_f}$	1000 cycles

Table A7.1: Example Calculations for AEC-Q102 Tests for Discrete Devices (continued)

Loading	Mission Profile Input	Stress Test	Stress Conditions	Acceleration Model (all temperatures in K, not in ℃)	Model Parameters	Calculated Test Duration	Q102 Test Duration
Humidity	Engine Non-operating: t_u = 119,400 hours (average engine off time over 15 years) RH_u = 75 % (average relative humidity in off mode) T_u = 30 ℃ (average junction temperature in engine off mode)	Wet High Temperature Operating Life (WHTOL) or High Humidity High Temperature Reverse Bias (H^3TRB)	RH_t = 85% (relative humidity in test environment) T_t = 85℃ (ambient temperature in test environment)	Hallberg-Peck $A_f = \left(\frac{RH_t}{RH_u}\right)^p \bullet \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$	p = 3 Reference Hallberg-Peck (1991) E_a = 0.9 eV Reference Hallberg-Peck (1991) k_B = 8.61733 x 10^{-5} eV/K (Boltzmann's Constant)	T_t = 413 h $t_t = \frac{t_u}{A_f}$	1000 h

Appendix 7a: Reliability Validation for LEDs

The progress in LED lighting technology is rapid. It is getting more and more common, that new kind of LED types and technologies are developed in parallel with lighting application. This makes it sometimes difficult to follow the Robustness Validation approach, described in Appendix 7.

For LEDs the use lifetime strongly depends on the kind of application. So interior lighting mostly has different requirements compared to exterior rear and exterior front lighting application. In addition also application for trucks may have different requirements compared to the majority of personal cars. The matrix here is seen to be a typical set of longtime reliability tests safeguarding the various lifetime reliability requirements. If reliability cannot be proven by the classical Robustness Validation approach, this set of tests can be chosen alternatively.

Test	Condition	RV-level 2	RV-level 1	RV-level 0
	Per AEC-Q102	Extreme long life exterior	Long life exterior	Interior and normal life exterior
HTOL 1	See test 5a	10000 hours	4000 hours	1000 hours
HTOL 2	See test 5b	10000 hours	4000 hours	1000 hours
PTC	See test 8	2500 cycles	2500 cycles	1000 cycles

Note:
Sample size: 30 parts (3 lots 10 pcs. each)
Failure criteria: 0 failures acc. to AEC-Q102 Appendix 5 allowed

RV level 1 & 2 are additional tests for robustness evaluation only. Passing tests, defined in Table 2 of base document AEC-Q102, (RV-level 0) qualifies the part already to AEC-Q102.

Especially but not limited for RV1 & RV2 it is strongly recommended to determine failure modes and acceleration parameter by the help of overstress tests. The following tests, derived from SAE/USCAR-33, are recommended:

- High Temperature Operating Life
  Tj = max. specified Tj +15°C (Tj +30 °C for Low and Mid Power LEDs < 1 W)
  I_F = 1.25x max. specified I_F (I_F = 1.5x for Low and Mid Power LEDs < 1 W)

- High Humidity & Temperature Operating Life
  85 °C 85% RH ambient
  I_F = 1.25x max. specified I_F (I_F = 1.5x for Low and Mid Power LEDs < 1 W)

- Power Temperature Cycle
  T_S = -40 °C to 125 °C
  10 min dwell, 20min transfer time
  2 min power ON / OFF each
  I_F = 1.3x max. specified I_F (I_F = 1.5x for Low and Mid Power LEDs < 1 W)

- Temperature Shock
  -55 °C/150 °C liquid/liquid
  15min dwell, <10 s transfer time

  Sample size: 78 parts (3 lots 26 pcs. each)
  Stress duration: 50% of samples size failed, 1500 hours / cycles maximum
  Perform Pre- and Post-Stress Electrical and Photometric Test and Pre-conditioning per AEC-Q102
  For failure criteria, follow AEC-Q102 Appendix 5
  Destructive Physical Analysis (DPA) shall be performed on 2 (failed) parts each test

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	Mar. 15, 2017	Initial Release.