JEDEC PUBLICATION

FOUNDRY PROCESS QUALIFICATION GUIDELINES – PRODUCT LEVEL

(Wafer Fabrication Manufacturing Sites)

JEP001-3A

(Revision of JEP001A, February 2014)

SEPTEMBER 2018

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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(Wafer Fabrication Manufacturing Sites)

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Foreword

The publication is divided into three parts, backend of line (JEP001-1A), transistor level (JEP001-2A), and product level testing (JEP001-3A). The document provides methodologies for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g., analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g., Cu/Low K interconnects or ultra-thin gate oxide.

Any qualification requirements beyond the minimum set are to be developed for the specific performance expected of the technology. The minimum set of measurements and the requirements for the qualification based on those measurements are to be determined between the foundry and its customers on an individual basis The process technology owner (foundry) will be required to document the details of specific testing unique to the process being qualified.

The guideline documents common best practices in the semiconductor industry and updated in accordance to advancement in the semiconductor industry and JEDEC bylaws of periodic reviews.

Introduction

This publication, was originally published as JP-001 entitled 'Foundry Process Qualification Guidelines', it was co-sponsored by JEDEC and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification methodologies. The JEDEC sponsoring committee is JC-14 through its JC-14.2 subcommittee on wafer level reliability.

This document encompasses and references a number of other standards and procedures, some of which are in a state of constant revision and update. While a case might be made for producing a lean, concise guideline that does not spell out specific procedures or requirements, the proposition of spelling out the essence of a comprehensive set of methodologies in one place has a practical value that outweighs the case for simplicity.(comment : the requirements are only spelled out in a number of cases. Best to be consistent and let the existing JEDEC specs speak for themselves)

The three parts: JEP001-1A, JEP001-2A, and JEP001-3A are described below. It is intended that each part references the appropriate test and requirement noting that some tests may be performed on the package level. This standard should be read alongside reliability requirements established between the supplier and customer.

The structure of the JEDEC JEP001 series as currently conceived is as follows:

Part 1 – Backend of line testing
Part 2 – Transistor-level testing
Part 3 – Product-level testing

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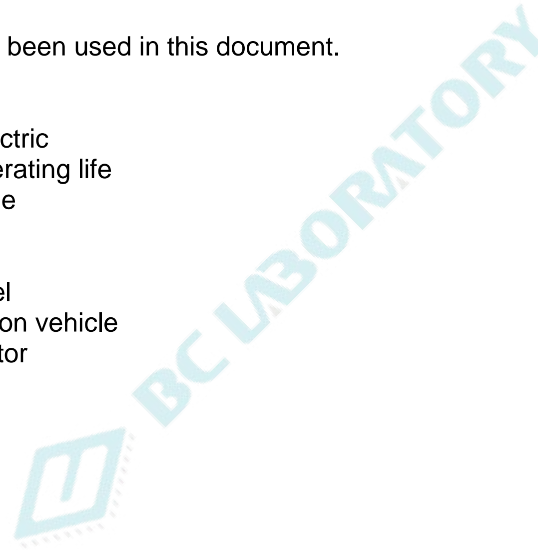
Acronyms

The following acronyms have been used in this document.



WLR: wafer level reliability
IMD: inter/intra-metal dielectric
HTOL: high temperature operating life
ESD: electrostatic discharge
HBM: human body model
MM: machine model
CDM: charged device model
TQV: technology qualification vehicle
PCM: process control monitor
FA: failure analysis

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FOUNDRY PROCESS QUALIFICATION GUIDELINES – PRODUCT LEVEL (Wafer Fabrication Manufacturing Sites)

(From JEDEC Board Ballot JCB-17-30, formulated under the co-sponsorship of the JC-14.2 Subcommittee on Wafer Level Reliability.)

1 Scope

This document describes package-level test and data methods for the qualification of semiconductor technologies. It does not give pass or fail values or recommend specific test equipment, test structures or test algorithms. Wherever possible, it references applicable JEDEC such as JESD47 or other widely accepted standards for requirements documentation.

There are two levels of qualification described. Level 1 is a pure process qualification intended to find reliability weaknesses. It primarily addresses technology wearout mechanisms through package or wafer level reliability tests on specially designed test structures.

Level 2 demonstrates the reliability of the process that corresponds to the reliability demands from projected or known applications. Level 2 testing can be implemented via the testing of a relevant functional technology qualification vehicle (TQV), including life test. The level 2 tests are described in clause 12. Other Reporting requirements (e.g., PCM data) are also included.

2 Quality system

It is the responsibility of the foundry to have the appropriate quality system in place with special emphasis on issues relating to equipment capability, maintenance and calibration, continuous improvement and process control. In particular, a functioning SPC methodology should be demonstrated for all key processes (see EIA/JEDEC EIA-557A). As a minimum the foundry will have ISO9001 certification. The ISO9001 audit results by a third party and subsequent corrective actions on deficiencies shall be made available to the customer upon request. For those supplying to automotive applications, the foundry may also have to demonstrate requirements from the IATF TS 16949 standard to meet the needs of these products.

3 Responsibilities

3.1 Level 1 qualification

The foundry is responsible for the design and implementation of the level 1 test vehicle (i.e., TESTCHIP). For the special case of a foundry customer driving process development, development of the level 1 test vehicle may be shouldered in whole or in part by the customer. The foundry shall fabricate the qualification silicon, execute the described level 1 tests and create the qualification report. The tests and qualification report may be done by the foundry or third party test vendor. The qualification requirements may be reduced for a derivative process, where the parent process has already been fully qualified at the same location.

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3.2 Level 2 qualification

In general, the foundry is responsible for the design and implementation of the Level 2 test vehicle (e.g., SRAM or pilot product). For the special case of a foundry customer driving process development, or where the customer requires TQV data before such a vehicle becomes available, development of the level 2 test vehicle may be shouldered in whole or in part by the customer. The foundry, customer or third party test vendor may execute the Level 2 (TQV) tests and requisite failure analysis. The foundry will be responsible for suggesting and implementing corrective action based on the failure analysis results. The qualification report shall adhere to the minimum reporting requirements and format described in this document.

While it is expected that a particular foundry methodology may differ from the methods outlined in this document, the wafer foundry should demonstrate to the customer that it has satisfactorily addressed all issues of interest. The wafer foundry should therefore provide a documented procedure and supporting data that provide an assessment of potential failure and wearout mechanisms.

3.3 Reporting Requirements

Specific reporting requirements are included for the tests catalogued in this document. General reporting requirements include appropriate signoff, archiving and revision control, and the inclusion of supporting documents as appropriate.

The level 1 qualification report shall include: (1) qualification plan, (2) description of the test vehicle including relevant test structure features and dimensions, (3) summary of test methods used, (4) pass/fail criteria and (5) test results, analysis and model parameters as described in this document.

The level 2 qualification report shall include: (1) qualification plan, (2) description of the technology qualification vehicle (TQV), (3) test description & specification, (4) pass/fail criteria (5) test results & analysis including failure rates and (6) FA results.

4 Sample size

In general, data should come from 3 non-consecutive wafer lots, although the use of more lots is not precluded. A wafer lot is a group of wafers processed as a batch through the same or matched equipment in the same processing interval, using the same or matched conditions, materials, and methods. Typical sample sizes per lot are given in the individual test descriptions. Where applicable, confidence limits for each test population should be calculated. A conservative estimate of 40 die per wafer was made in determining sample size for tests that required the usage of all dies on the wafer.

5 Use of packages

Packages with a wire-bonded die that are capable of higher temperatures are generally used for testing of the technology qualification vehicle (TQV) or pilot product. A qualification report for the standard wire-bonding process should be included. Advanced packaging (e.g., BGA, flip-chip or chip-scale) may be substituted where applicable. This, in combination with TC and THB tests will demonstrate the assembly capability of this wafer fab process.

Side brazed ceramic packages are generally required for process wear-out tests performed at package-level at Temperatures greater than 155°C. Consequently, wafer level testing is recommended wherever possible.

All references to temperature in the following sections imply junction temperature unless otherwise specified.

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6 Reference documents

6.1 Industry standard documents

The following reference documents contain provisions that, through reference in this text, constitute provisions of this document. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based in this publication are encouraged to investigate the possibility of applying the most recent editions of the reference documents indicated below. For undated references, the latest editions of the reference document referred to applies. Check the JEDEC website at http://www.jedec.org.

6.1.1 Reliability assessment methodology

JEDEC JEP70, *Quality and Reliability Standards and Publications.*

JEDEC JEP132, *Process Characterization Guidelines.*

JEDEC JEP143, *Solid State Reliability Assessment and Qualification Methodologies.*

JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.*

JEDEC JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms.*

JEDEC JESD94 Application Specific Qualification Using Knowledge Based Test Methodology

JEDEC JESD659, *Failure-Mechanism-Driven Reliability Monitoring.*

JEDEC JEP131, *Process Failure Mode and Effects Analysis (FMEA).*

6.1.2 Endurance tests

IPC/JEDEC J-STD-020, *Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices.*

JEDEC JESD22-A101, *Steady State Temperature Humidity Bias.*

JEDEC JESD22-A104, *Temperature Cycling.*

JEDEC JESD22-A108, *Temperature, Bias and Operating Life.*

JEDEC JESD22-A110, *Highly Accelerated Stress Test (HAST).*

JEDEC JESD22-A113, *Preconditioning of Surface Mount Devices prior to Reliability Testing.*

JEDEC JESD47, *Stress-Test Driven Qualification of Integrated Circuits.*

JEDEC JESD50, *Special Requirements for Maverick Product Elimination.*

JEDEC JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.*

JEDEC JESD85, *Methods for Calculating Failure Rates in Units of FITs.*

6.1.3 Electrostatic discharge tests

JESD22-A115, *Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM).*

JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds for Microelectronic Components.*

ANSI ESD S5.1, *Electrostatic Discharge Sensitivity Testing – Human Body Model.*

ANSI ESD STM5.2, *Electrostatic Discharge Sensitivity Testing – Machine Model.*

ANSI ESD S5.3.1, *Charged Device Model (CDM) – Component Level.*

ANSI/ESDA/JEDEC JS-001-2012, *ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM)*

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6.1.4 Latchup test

JEDEC JESD78, *IC Latch-Up Test.*

6.1.5 E-Test Parameters

ASTM F616-86, *Standard Test Method for Measuring MOSFET Drain Leakage Current.*
ASTM F617-86, *Standard Test Method for Measuring MOSFET Linear Threshold Voltage.*
ASTM F1096-87, *Standard Test Method for Measuring MOSFET Saturated Threshold Voltage.*

6.1.6 Quality standards

EIA-557, *Statistical Process Control Systems.*
EIA-670, *Quality System Assessment.*
ISO 9001:2000, *Quality Management Systems – Requirements.*
JESD671, *Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems).*

6.2 Selected references

Meeker, Q.A. and L.A. Escobar, *Statistical Methods for Reliability Data,* John Wiley, 1998.

Tobias, P.A. and D.C. Trindade, *Applied Reliability,* 2nd Ed., CRC Press, 1995.

Nelson, Wayne, "Accelerated Testing: Statistical Models, Test Plans, and Data Analyses", in *Wiley Series in Probability and Mathematical Statistics-Applied Probability,* John Wiley, 1990.

Amerasekera, E.A. and F.N. Najm, *Failure Mechanisms in Semiconductor Devices,* 2nd Ed., John Wiley, 1997.

Ohring, Milton, *Reliability and Failure of Electronic Materials and Devices,* Academic Press, 1998.

Yue, John, "Reliability", in C.Y. Chang and S.M. Sze (eds.), *ULSI Technology,* McGraw-Hill, 1996, Chapter 12.

Takeda, E. et al, *Hot-Carrier Effects in MOS Device,* Academic Press, 1995.

Amerasekera, E.A. and Charvaka Duvvury, *ESD in Silicon Integrated Circuits,* John Wiley, 1996.

IRPS Conference Proceedings and Tutorials are an excellent source of information on current test methodologies and reliability models. (Web site www.irps.org)

Microelectronics Reliability, Pergamon Press. This journal publishes the proceedings of ESREF, the European equivalent of IRPS, along with frequent review papers.

Abadeer, W.W., IEEE Transactions on Device and Materials Reliability, Vol. 1, No. 1, March 2001, *Reliability Monitoring and Screening Issues With Ultrathin Gate Dielectric Devices.*

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7 Qualification test summary table

Section	Procedure	JEDEC Reference Standard(s)	Other Standards	Qual or Eng
8.1	Long Term Life Test (HTOL)	JESD22-A108, JESD47, JESD74, JESD85		Q
8.2	Early Life Test	JESD22-A108, JESD47, JESD74, JESD85		Q
8.3	Temperature Cycling (TC)	JESD22-A113, JESD22-A104, JEP122		Q
8.4	Temperature Humidity Bias (THB) or Highly Accelerated Stress Test (HAST)	JESD22-A113, JESD22-A101, JESD22-A110		Q
8.6	ESD Characterization	JESD22-A114, JESD22-A115, JESD22-C101	ANSI/ESD: STM5.1, STM5.2 & STM5.3	Q
8.7	Latchup Characterization	JESD78		Q
9.1	Process Control Monitor (PCM) Characterization	JEP132	ASTM: F616-86, F617-86 & F1096-87	Q
10.1	Construction Analysis	None		Q

8 Technology qualification vehicle (TQV) tests

An appropriate technology qualification vehicle - SRAM or circuit of equivalent complexity is used to get a first look at the expected long-term failure rate of the process. Recommended SRAM sizes appear below and are based on SRAMs populated with a bit design and layout density expected to be typical at the respective lithographic node. For other qualification vehicles (e.g., ASIC), a number of circuits providing an equivalent density should be used.

Lithographic Node (nm)	SRAM size (Mb)
180	2
150	4
130	8
90	16
65	32
45/40	64
32/28	128
22/20	256
15	512

NOTE 1 An SRAM is an excellent vehicle where the primary concern is defect density. However, it has far too uniform a topology to be a good overall qualification vehicle in cases where divergent topologies may give rise to specific reliability concerns. Other vehicles may need to be used to provide a more thorough evaluation.

NOTE 2 Evaluations driven by defect density require a larger number of samples where the vehicle size is reduced. For example, a 50% reduction in SRAM size would drive a 2x increase in the number of samples needed for a comparable measurement on a per circuit basis.

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8.1 Long term life test

The usefulness of a life test is dependent on an assessment of the dominant failure modes, as determined from a prior thorough analysis of failure modes (FMEA). See JEDEC publication JEP131.

8.1.1 Operating life test requirements

Reference procedures	JESD22- A108, *Temperature, Bias, and Operating Life.* JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.* JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.* JESD85, *Methods for Calculating Failure Rates in Units of FITs.* JEP131, *Process Failure Mode and Effects Analysis (FMEA).*
Vehicle	Appropriate technology qualification vehicle (TQV) in component form
Method	• As Per JESD22-A108 Bias Life with 125 °C < T_J < 150 °C. • Full Functional Burn-in with F > 100 kHz • Voltage – see discussion under per circuit bias configuration • Total stress hours: 1000 -0/+8 hours at minimum V_{CC_STRESS} Or scaled from 1000 hrs. based on acceleration for $V_{CC_STRESS} > V_{CC_OPERATING}$ and 500 -0/+8 hours at minimum under any V_{CC_STRESS} • Test Points at 0, 48, 168, 504 and 1000 hours (or appropriately scaled to the end of stress) A higher ambient temperature may be used to reduce the required total stress hours. Care should be taken to ensure that the case and junction temperatures are within the applicable range for the process and package. <u>DRIFT ANALYSIS (optional)</u> For a statistically significant sample of devices per lot, serialize devices - Option #1: Take read and record data of key parameters drift (most sensitive to drift) at 0, 48, 168 and 500 - Option #2: Take read and record data of key parameters drift at suitable intervals - Analyze data to determine potential drift and report in tabular or graphical form for each parameter
Circuit bias configuration	$V_{CC_STRESS} = \lambda\ V_{CC_OPERATING}$, where V_{CC_STRESS} must not exceed the device functional limits The minimum λ allowed is 1, but may range up to that tolerated for a stress period without artificially damaging the devices under test.. NOTE 1 Unless otherwise specified, the operating voltage is the maximum operating voltage specified for the device. NOTE 2 The voltage acceleration model should be obtained from specific failure data for the product under test. NOTE 3 The nomenclature V_{CC}, or alternatively V_{DD}, refers to the voltage(s) applied to the power supply pins.
Criteria For failure	Full Functional Test and, where appropriate, I_{DDQ} and Leakage Tests.
Failure analysis	Root cause analysis should be pursued for all failure types to substantiate models applied and as an opportunity for improvement actions.

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8.1.1 Operating life test requirements (cont'd)

Model to be used	Total acceleration factor AF(T,V) = AF(T) * AF(V) a) Temperature Acceleration, AF(T) - Arrhenius model for temperature acceleration factor (AFT): $AFT = \exp(E_A/k[(1/T_{USE})-(1/T_{STRESS})])$ - T_{USE} & T_{STRESS} are junction temperatures in kelvin. - k = Boltzman's constant = 8.62E-05 eV/K - Activation energy is to be determined by failure mechanism. (see JEP122 as one reference) or as a composite behavior for the population (with justification). b) Voltage Acceleration, AF(V) - Correct voltage acceleration factor is to be derived for the product being stressed. If the voltage acceleration is defect driven, the following model may be used: $AFV = \exp(\alpha\ (V_{CC_STRESS} - V_{CC_OPERATING})$ NOTE 1 For the purpose of calculating the temperature acceleration factor, T_{USE} is typically NOT the maximum operating temperature. Rather, it represents an average junction temperature over the life of the product. Typical values of T_{USE} are 55 °C (consumer), 70 °C (commercial), and 85 °C (industrial). NOTE 2 There is no universally agreed value of E_A to be used for temperature acceleration of product failures. In the absence of a reliable model, a value of E_A = 0.7 eV has historically been used. It is the responsibility of the technology owner to demonstrate that a conservative model is used.
Sample size	Approximately equal numbers of samples shall be selected from each of (at least) three lots. The sample size shall be sufficient to demonstrate the required failure rate under the applicable time distribution model: 1. **<u>Decreasing or generalized distribution of failures</u>**: Use a Weibull model; other models may apply with justification. This can often mean normalizing end of stress data to an equivalent use condition and lifetime to arrive at the appropriate device failure rate. JESD74 provides reference on this type of analysis. 2. **<u>Constant distribution of failures</u>**: The FIT rate should be calculated using Chi-Square statistics at 60% confidence limits (see JESD85). $\lambda = \chi^2(x,\nu) / (2N \cdot AF \cdot \mathbf{t}_{STRESS})$ where: $\chi^2(x,\nu)$ = Chi Square at (x, ν), from Chi Square tables x = (1-C.L.) and ν = (2r+2) C.L. = Confidence limit r = # of rejects N = Total sample size AF = Acceleration factor $\mathbf{t}_{STRESS}$ = Total stress time
Merit number	- % Failures for each lot at each read-out point. - Failure rate with an appropriate failure distribution model. -
Other data required	Standard Lot Data

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8.1.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. % Failures for each lot at each read-out point.
5. Target defect density and failure rate requirements.
6. Calculated failure rates at the specified read-points. NOTE: The earliest part of the failure distribution (< 48 hours if no voltage acceleration or equivalent at higher voltages) are excluded in the calculation of long term operating life. Specify the criteria and method of calculating failure rate.
7. Appropriate failure analysis reports.
8. Corrective actions taken.
9. Drift analysis results. (optional)

8.2 Early life test

An appropriate technology qualification vehicle (TQV) is to be used to get a first view on the expected infant mortality rate of the process. The life period of interest is typically the first year or less. It may be possible to utilize early data from the long term life test to fulfill the objective of this section.

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8.2.1 Early life test requirements

Reference procedure	JESD22- A108, *Temperature, Bias, and Operating Life.* JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.* JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.* JESD85, *Methods for Calculating Failure Rates in Units of FITs.*
Vehicle	Appropriate technology qualification vehicle (TQV) in component form
Method	Per JESD22- A108 Bias Life with • 125 °C < Tj < 150 °C, 48 hours • Dynamic Burn-in with F > 100 kHz • Voltage – see discussion under per circuit bias configuration • Test Points: 0 & 48 hours. Intermediate readout points may be added as required. A higher ambient temperature may be used to reduce the required total stress hours. Care should be taken to ensure that the case and junction temperatures are within the applicable range for the process and package.
Circuit bias configuration	$V_{CC_STRESS} = \lambda V_{CC_OPERATING}$, where • V_{CC_STRESS} is at least V_{CCMAX} (V_{CCMAX} is often 1.1 X $V_{CC_NOMINAL}$) • V_{CC_STRESS} must not exceed the device functional limits The minimum λ allowed is 1, but may range up to that tolerated for a stress period without artificially damaging the devices under test.. NOTE 1 Unless otherwise specified, the operating voltage is the maximum operating voltage specified for the device. NOTE 2 The voltage acceleration model should be obtained from specific failure data for the product under test. NOTE 3 The nomenclature V_{CC}, or alternatively V_{DD}, refers to the voltage(s) applied to the power supply pins
Criteria for failure	Full Functional Test and, where appropriate, I_{DDQ} and Leakage Tests.
Model to be used	Total acceleration factor AF(T,V) = AF(T) * AF(V) a) Temperature Acceleration, AF(T) Arrhenius model for temperature acceleration factor (AFT) $AFT = \exp(E_A/k[(1/T_{USE})-(1/T_{STRESS})])$ - T_{USE} & T_{STRESS} are junction temperatures in kelvin. - k = Boltzman's constant = 8.62E-05 eV/K - Activation energy is to be determined by failure mechanism. (see JEP122 as one reference) or as a composite behavior for the population (with justification). b) Voltage Accelertion, AF(V) Absent an experimentally-validated, alternate, the following model is recommended: $AFV = \exp[\gamma_V * (V_{STRESS} - V_{USE})]$ - γ_V is a voltage acceleration parameter - The values of γ_V is determined experimentally and may vary by failure mechanism. - If $V_{CC_STRESS} = V_{CCMAX}$, then AFV = 1
Sample size	Approximately equal numbers of samples shall be selected from each of three lots (minimum). The sample size shall be sufficient to demonstrate the required early failure rate
Merit number	1. Fraction failure for each lot at each readout point 2. Total failures in DPPM (defective parts per million) or The early failure rate derived from accelerated stress and quoted at a normalized use condition and early life point.
Other data required	Standard lot data

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8.2.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. % Failures for each lot at every readout point.
5. Total failures in DPPM (defective parts per million) at a projected number of use hours (e.g., 3000 hours) under a stated use conditions of temperature, voltage, and any other primary variables
6. JESD74 describes appropriate interpretation of data to assess the early life failure rate. Included are descriptions for interpreting data when
   - the failure rate is decreasing (This is often the case for early life)
   - the failure rate is constant (This can be rare where defects are a factor in early reliability.)

   Where the stress readout and the early life point of interest are not equivalent, proper interpretation methodology is especially critical.

8.3 Temperature cycling test

8.3.1 Temperature cycling test requirements (package level)

Reference procedures	JESD47, *Qualification Methods* JESD22-A104, *Temperature Cycling* J-STD-020, *Moisture level preconditioning* JESD22-A113, *Preconditioning of Surface Mount Devices Prior to Preconditioning*
Test structures	Appropriate technology qualification vehicle
Vehicle	Plastic Package or other appropriate package.
Method	Preconditioning per appropriate MSL Level per J-STD-020 and JESD 22-A113 Temperature Cycle per JESD47
Circuit bias configuration	None (This test is unbiased.)
Criteria for failure	Per JESD47
Model to be used	See JEP122
Sample size	Follow option (a) or (b): a) A minimum of 231 DUTs from three lots with no more than 90 DUTs from any one lot, a) 45 parts from 3 lots for an initial foundry qual, with the understanding that data from later product quals and/or quality monitor stress can be summed up to meet the 231 total.
Merit number	- % Failure. - Distribution Analysis if failures are present
Other data required	Standard Lot Data

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8.3.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Sample size for each lot and the number of failures at each readout point
5. Percent failure.
6. Description of the plastic package (type, # pins, dimensions, lead-frame)

8.4 Temperature-humidity-bias (THB)/highly accelerated stress test (HAST)

Either THB or HAST is required.

8.4.1 THB/HAST test requirements

Reference procedures	JESD47, *Qualification Methods.* J-STD-020, *Moisture level preconditioning.* JESD22-A113, *Preconditioning of Surface Mount Devices Prior to Preconditioning.* JESD22-A101, *Steady State Temperature Humidity Bias Life Test.* JESD22-A110, *Highly Accelerated Stress Test (HAST).*
Test conditions	Static bias = V_{CCMAX} (typically 1.1 V_{CCNOM}) Biasing guidelines: See JESD22-A101 (THB) or JESD-A110 (HAST) • THB: 85 °C/85%RH, 1000 hours • HAST: 130 °C, 85%RH, 96 hours. For interim readouts, devices should be returned to stress within the time specified in JESD22-101 or JESD22-110.
Test structures	Appropriate technology qualification vehicle. If a dc test structure is designed it should be set up for zero power dissipation under bias and maximum rated voltage for the technology. (Functional test structures will have transistor leakage)
Vehicle	Plastic package or other appropriate package.
Method	Preconditioning per appropriate MSL Level per JESD22_A113 Stress in either THB or HAST per JESD47
Model to be used	See JEP122
Sample size	Follow option (a) or (b): a) A minimum of 231 DUTs from three lots with no more than 90 DUTs from any one lot, b) 45 parts from 3 lots for an initial foundry qual, with the understanding that data from later product quals and/or quality monitor stress can be summed up to meet the 231 total.
Merit number	% Failure
Other data required	Standard lot data

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8.4.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Sample size for each lot and the number of failures at each readout point
5. Total failures in DPPM (defective parts per million)

8.5 Detailed yield results

Reference procedure	None
Test parameters	Full Functional Test and I_{DDQ} and Leakage Tests
Test structures	Appropriate technology qualification vehicle
Vehicle	Wafer Probe
Method	NA
Model to be used	Foundry Will specify Yield Model
Sample size	12 wafers from each of 6 lots
Defect density	Defects per square centimeter
Other data required	1) Area of SRAM or other qualification vehicle 2) # of Critical Layers Used 3) Site location information relative to edge exclusion zone

8.5.1 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Number of devices tested, devices passed and percent yield for each wafer tested.
5. Defect density per square cm.

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8.6 ESD characterization

The technology qualification vehicle (TQV) is used to get a first look at the ESD robustness of the process and product (especially I/O) design. As a minimum, human body model (HBM) test data should be collected. The inclusion of charged device model (CDM) data is highly recommended. The collection of machine model (MM) data is not considered essential (see JEP155).

8.6.1 ESD tests

Reference procedure	JS-001 Human Body Model ESD Test Method JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds for Microelectronic Components* JESD47.
Test parameters	Full Functional Test and Parametric (e.g., I_{DDQ} and Leakage) Tests
Test structures	I/O and power pins of appropriate technology qualification vehicle
Vehicle	Packaged TQV
Method	Per JESD47
Model to be used	None
Sample size	Per JESD47
Failure criteria	Per JESD47
Merit number	Voltage level or classification per respective test method
Other data required	Tester waveforms

8.6.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & test coverage, test speed (frequency), I_{DDQ} limits.
4. HBM ESD classification.

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8.7 Latch-up characterization

The technology qualification vehicle (TQV) is used to get a first look at the latch-up immunity of the process and ruggedness of the product design. This is a package level test.

8.7.1 Latchup test

Reference procedure	JESD78, *IC Latch-Up Test.*
Test parameters	Full Functional Test and Parametric (e.g., I_{DDQ} and Leakage) Tests
Test structures	I/O and power pins of appropriate technology qualification vehicle
Vehicle	Packaged TQV
Method	Method per specification Per JESD78 and JESD47 if appropriate per technology or device under consideration
Model to be used	None
Sample size	Per JESD78 and JESD47 if appropriate per technology or device under consideration
Failure criteria	Per JESD78 and JESD47 if appropriate per technology or device under consideration
Merit number	Class (room and max temperature) Maximum passing current trigger and voltage trigger levels
Other data required	Tester waveforms

8.7.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Latch-up test conditions: Trigger test conditions, test temperature, failure criteria.

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Annex A (informative) Differences between revisions

A.1 Differences between JP001-3A and JEP001A

The following list briefly describes most of the changes made to entries that appear in this publication, JP001-3A, compared to its predecessor, JP001A (February 2014).

Clause	Description of Change
All	JEP001A – split into three parts, JEP001-1A Backend of Line, JEP001-2A, FEOL END Transistor Level, and JEP001-3A Product Level. .

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Standard Improvement Form JEDEC JP001-3A

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1. I recommend changes to the following:
   - [ ] Requirement, clause number ____________
   - [ ] Test method number ____________ Clause number ____________

   The referenced clause number has proven to be:
   - [ ] Unclear [ ] Too Rigid [ ] In Error
   - [ ] Other ____________

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

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