JEDEC STANDARD

High Temperature Storage Life

JESD22-A103E

(Revision of JESD22-A103D, December 2010)

OCTOBER 2015

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD A103E

HIGH TEMPERATURE STORAGE LIFE

(From JEDEC Board Ballot JCB-15-48, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices.

The high temperature storage test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). Thermally activated failure mechanisms are modeled using the Arrhenius Equation for acceleration. During the test, accelerated stress temperatures are used without electrical conditions applied. This test may be destructive, depending on time, temperature and packaging (if any).

2 Reference documents (informative)

JEP122, *Failure Mechanisms and Models for Semiconductor Devices.*

JESD22-A113, *Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing.*

JESD22-B101, *External Visual.*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits.*

JESD94, *Application Specific Qualification Using Knowledge Based Test Methodology.*

J-STD-020, Joint IPC/JEDEC Standard, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices.*

3 Apparatus

3.1 High temperature storage chambers

The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature over the entire sample population under test.

3.2 Electrical test equipment

Electrical equipment capable of performing the appropriate measurements for the devices being tested, including write and verify the required data retention pattern(s) for nonvolatile memories.

4 Procedure

4.1 High temperature storage conditions

The devices under test shall be subjected to continuous storage at one of the temperature conditions of Table 1.

Table 1 — High temperature storage conditions

Condition A: +125 (-0/+10) °C
Condition B: +150 (-0/+10) °C
Condition C: +175 (-0/+10) °C
Condition D: +200 (-0/+10) °C
Condition E: +250 (-0/+10) °C
Condition F: +300 (-0/+10) °C

NOTE CAUTION should be exercised when selecting an accelerated test condition since the accelerated temperature used may exceed the capabilities of the device and materials, thereby inducing (overstress) failures that would not occur under normal use conditions.

As a minimum the following items should be taken into consideration:

1) Melting point of metals present, especially solder. Degradation of metals including metallurgical interfaces.
2) Package degradation. For example: glass transition temperature and thermal stability (in air) of any polymeric materials.
3) Moisture rating of package (per J-STD-020).
4) Temperature limitations of silicon devices. For example: charge loss in nonvolatile memories.
5) Test conditions (temperature, time) should be selected to cover the acceleration of the corresponding failure mechanism and the anticipated lifetime (operational time) of the device.

4.1 High temperature storage conditions (cont'd)

Qualification documents such as JESD47 and reliability monitoring agreements should provide stress durations for the stress conditions stated in Table 1. 1000 hours is a typical duration for condition B. Other conditions and durations may be used as appropriate. JESD47[1] also recommends that some package styles be subjected to SMT reflow simulation prior to stress.

Alternatively, application of a knowledge-based test method that reconciles use condition data (JESD94) and an understanding of reliability models and failure mechanisms (JEP122) can provide the test durations for any selected stress condition in Table 1.

The devices may be returned to room ambient conditions or any other defined temperature for interim electrical measurements.

4.2 Measurements

Unless otherwise specified, interim and final electrical test measurements shall be completed within 168 hours after removal of the devices from the specified test conditions. Interim measurements are optional unless otherwise specified. The time window need not be met if verification data for a given technology is provided. If the final readpoint time window is exceeded then the units may be restressed for the same amount of time that the window is exceeded.

The electrical test measurements shall consist of parametric and functional tests specified in the applicable procurement document. For nonvolatile memories, the data specified data retention pattern must be written initially, and then subsequently verified without re-writing.

4.3 Failure criteria

A device will be considered a high temperature storage failure if parametric limits are exceeded, or if functionality cannot be demonstrated under nominal and worst-case conditions, as specified in the applicable procurement document. For nonvolatile memories, the specified data retention pattern shall be verified before and after storage. A margin test may be used to detect data retention degradation.

Mechanical damage, such as cracking, chipping, or breaking of the package, (as defined in JESD22-B101) will be considered a failure, provided that such damage was not induced by fixtures or handling and it is critical to the package performance in the specific application.

Cosmetic package defects and degradation of lead finish, or solderability are not considered valid failure criteria for this stress.

[1] From Table 2 of JESD47 - Preconditioning to JESD22A113 is recommended, specifically for wirebonded products qualified to Pb-free reflow profiles. Moisture soak as part of the preconditioning is optional.

5 Summary

The following details shall be specified in the applicable procurement document.

a) Electrical test measurements, failure criteria and specifications

b) Sample size and number of failures (specify zero if none observed)

c) Condition per Table 1, and duration of stress

d) Interim electrical test measurements, if required

e) Nonvolatile memory data retention pattern (for appropriate devices)

Annex A (informative) Differences between JESD22-A103E and JESD22-A103D

This annex briefly describes most of the changes made to entries that appear in this standard, JESD22-A103E, compared to its predecessor, JESD22-A103D (December 2010). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of change
2	Added JEP122 and JESD94, as well as JESD22-A113 which is mentioned in a note.
4.1	Modified text to emphasize that stress duration requirements are stated in qualification documents, such as JESD47 or in customer agreements, and not in this test method. Also added a reference that JEP122 and JESD94 can be used to determine appropriate stress duration.
5	Modified item C to remove reference of stress duration requirement.

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

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_____

3. Other suggestions for document improvement:

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