JEDEC STANDARD

Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

JESD22-A113H

(Revision of JESD22-A113G, October 2015)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD A113H

PRECONDITIONING OF NONHERMETIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING

Foreword

This document provides an industry standard test method for preconditioning packaged devices that is representative of a typical industry multiple solder reflow operation.

Introduction

The typical use of surface mount devices (SMD) involves subjecting the SMDs to elevated temperatures during board assembly, which, by itself or combined with moisture in the package can induce internal package damage that could be a reliability concern. Preconditioning of SMD packages is used to simulate the effects of board assembly prior to reliability testing. This allows reliability testing at the packaged device level on as shippable products with a board assembly simulation. During preconditioning, test samples are subjected to temperature cycling (optional), dry bake, moisture soaking, solder reflow simulation, flux, rinse, dry, and electrical test before reliability testing.

This test method references the reflow profiles stated in J-STD-020. If a packaged device is not able to withstand the full thermal profile as stated in J-STD-020, J-STD-075 should be used to evaluate and classify process sensitivities.

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TEST METHOD A113H

PRECONDITIONING OF NONHERMETIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING

(From JEDEC Board ballot JCB-16-52, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This Test Method establishes an industry standard preconditioning flow for nonhermetic solid state SMDs that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow).

NOTE For good correlation of results between moisture/reflow-induced stress sensitivity testing (per J-STD-020 and JESD22-A113) and actual reflow conditions used, identical temperature measurements by both the SMD manufacturer and the board assembler are necessary. Therefore, it is recommended that the package temperature at the top center of the package be determined during assembly board reflow profile setup, to ensure that it does not exceed the evaluation temperature based on package thickness and volume as stated in J-STD-020.

2 Normative reference

IPC/JEDEC J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

IPC/JEDEC J-STD-033, *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*

ECIA/IPC/JEDEC J-STD-075, *Classification of Non-IC Electronic Components for Assembly Processes*

JESD22-A104, *Temperature Cycling*

JESD625, *Requirements for Handling Electrostatic Discharge Sensitive (ESD) Devices*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*

JESD94, *Application Specific Qualification Using Knowledge Based Test Methodology*

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3 Apparatus

This test method requires use of the following equipment.

3.1 Temperature and humidity chamber

Moisture chamber(s) capable of operating at 85 °C/85% RH, 85 °C/60% RH, and 30 °C/60% RH. Within the chamber working area, temperature tolerance must be ±2 °C and the RH tolerance must be ±3% RH. A chamber with 60 °C/60% RH capability is optional for accelerated soak conditions (See J-STD-020).

3.2 Solder reflow equipment

a) (Preferred) - Full Convection reflow system capable of maintaining the reflow profiles required by this standard.

b) Infrared (IR)/Convection solder reflow equipment capable of maintaining the reflow profiles required by this standard. It is required that this equipment use IR to heat only the air and not directly impinge upon the SMD packages under test.

NOTE The moisture/reflow and process sensitivity classification test results are dependent upon the package body temperature (rather than the reflow carrier and/or package terminal temperature).

3.3 Optical microscope

Optical Microscope (40x for external visual exam).

3.4 Electrical test equipment

Electrical test equipment capable of performing room temperature dc and functional tests.

3.5 Bake oven

Bake oven capable of operating at 125 +5/-0 °C.

3.6 Temperature Cycle Chamber

Temperature Cycle Chamber capable of operating, as a minimum, over the range of -40 °C (or lower) to 60 °C (or higher) per JESD22-A104. This equipment is only required if optional Step 4.3 is used.

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4 Test procedure

Using similar SMDs, it is recommended that the moisture sensitivity level (MSL), per J-STD-020, be determined before starting the preconditioning sequence to establish which moisture soak condition is appropriate, i.e., likely to pass. If the MSL level is not known then other relevant moisture evaluation data may be consulted, or an arbitrary selection may be made. Multiple moisture soak conditions can also be run to determine a passing level. However, the soak condition used must be consistent with the floor life information in J-STD-020.

Reflow requirements are provided for both Pb-free and legacy SnPb conditions and should be used based on the intended end use of the SMD. The same package may have different MSL levels depending on whether the SnPb or Pb-free reflow is used.

Some SMDs with a unique construction or materials may have limitations independent of moisture exposure that are strictly due to the thermal profile stated in J-STD-020 and may not be able to fully meet one or several of the temperature and/or duration requirements of the reflow profile. Some SMDs may have other limitations due to other assembly processes, such as exposure to chemicals. For those SMDs with thermal and/or other process limitations follow the process sensitivity classification stated in J-STD-075 to identify the appropriate process sensitivity level (PSL) rating.

For example, if a SMD cannot meet its required peak temperature based on its volume and thickness, then the peak temperature of the profile used for the preconditioning must be changed based on the value stated by its PSL classification. Thus if the SMD should be subjected to 260 °C, but its PSL rating is R6, the peak temperature used for preconditioning shall be 250 °C.

Similar to MSL, if the PSL level is not yet determined, relevant evaluation/engineering data may be used to generate the initial profile parameters. If the SMD passes the subsequent qualification testing, then the PSL rating will be based on the chosen parameters used for preconditioning; however, if there are fails that are deemed to be due to the thermal exposure of the preconditioning flow, requalification is required with reduced profile conditions that allow the SMD to pass the qualification requirements.

At all times the test parts should be handled using proper ESD procedures in accordance with JESD625.

Refer to Annex A for the typical test flow.

NOTE If the preconditioning sequence is being performed by the semiconductor manufacturer, steps 4.1, 4.2, and 4.4 are optional since they are the supplier's risks. If the preconditioning sequence is being performed by the user, steps 4.7 through 4.9 are optional.

4.1 Initial electrical test

Perform electrical and/or functional test to verify that the SMDs meet the room temperature data sheet specification. Replace any test samples that fail to meet this requirement.

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4 Test procedure (cont'd)

4.2 Visual inspection

Perform an external visual examination under 40X optical magnification to ensure that no samples with external cracks or other damage are used in this test method. If mechanical rejects are found, corrective action must be implemented in the manufacturing process and a new sample must be drawn from product that has been processed with the corrective action.

4.3 Temperature cycling

Perform five (5) cycles of temperature cycle from -40 °C (or lower) to 60 °C (or higher) to simulate shipping conditions. Acceptable alternative test conditions and temperature tolerances are A through I, L through N, and T as defined in Table 1 of JESD22-A104, Temperature Cycling. This step is optional based on product requirements.

4.4 Bake out

Bake the samples for 24 hours minimum at 125 +5/-0 °C. This step is intended to remove all moisture from the package so that it will be "dry."

NOTE 1 This time/temperature may be modified if desorption data on the particular SMD being preconditioned shows that a different condition is required to obtain a "dry" package. Refer to J-STD-020 for procedures on running absorption and desorption curves.

NOTE 2 If the SMD cannot be subjected to a bake at 125 °C for 24 hours or longer, then use a lower temperature condition with a longer duration to ensure that all moisture is removed. See J-STD-033 for alternative bake conditions and durations that are equivalent.

4.5 Moisture Soak

Place samples in a clean, dry, shallow container so that the package bodies do not touch or overlap each other. Submit each sample to the appropriate moisture soak requirements shown in J-STD-020. The moisture soak should be initiated within 2 hours of bake.

NOTE The moisture soak is optional for SMDs (e.g., Flip Chip / bumped die devices, etc.) where moisture absorption data is available showing the particular SMD being preconditioned either does not absorb moisture or desorption is so fast that the preheat portion of the reflow cycle will remove all moisture. Alternatively, the moisture soak can be abbreviated to the point in time where saturation occurs based on available absorption data. Refer to J-STD-020 for procedures on running absorption and desorption curves.

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4 Test procedure (cont'd)

4.6 Reflow

Not sooner than 15 minutes and not longer than 4 hours after removal from the temperature/humidity chamber, subject the sample to 3 cycles (See NOTE 1) of the appropriate reflow conditions. The reflow conditions are defined in J-STD-020. If the timing between removal from the temperature/humidity chamber and initial reflow cannot be met then the parts must be rebaked and resoaked according to 4.4 and 4.5.

NOTE 1 The 3 reflow cycles represent the following:
- Cycle 1 - the first pass of a Double-Sided, Double-Pass (DSDP) assembly reflow process.
- Cycle 2 - the second pass of a DSDP assembly reflow process.
- Cycle 3 - rework of a near neighbor on the assembly where the SMD being classified experiences reflow-like temperatures.

NOTE 2 For SMDs classified per J-STD-075 that cannot be subjected to 3 reflows, only perform the number of reflows for which the SMD is classified.

NOTE 3 If the reflow cycle regimen is not representative for the SMD being classified, refer to JESD94 for application specific qualification guidance. The following is an example of an application that would require an addition reflow cycle. SMDs that are placed directly next to a CPU in an LGA socket or on the underside of the PWB from an LGA socket (e.g., power management devices) may see 4 reflow cycles due to rework of the LGA socket. In that case, evaluation of 4 reflow cycles may be necessary to account for the total thermal exposure. Reflow cycle 3 would represent the removal of a damaged LGA socket and reflow cycle 4 would simulate the attaching of the replacement socket.

The sample parts shall be cooled sufficiently (preferably back to room temperature) between reflow cycles so that the reflow temperatures/times of the samples are not affected on the subsequent reflow cycles.

Reflow practices shall be sufficient to ensure that all sample parts, in each reflow cycle, will meet the appropriate reflow profile requirements of J-STD-020.

SMDs intended for use in a "Pb-free" assembly process shall be evaluated using the "Pb-free" reflow temperature whether or not the SMD is Pb-free.

If parts are reflowed in other than the normal assembly reflow orientation (i.e. live bug/dead bug) the damage response should be correlated.

The reflow oven should be loaded with the same configuration or be verified to have an equivalent thermal load when running preconditioning as was used to develop the reflow profile.

The reflow profiles in J-STD-020 are only for classification and preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in J-STD-020.

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4.6 Reflow (cont'd)

4.6.1 Solder attachment after reflow

If reliability testing is to be performed in a second level configuration, one of the reflow cycles may be used to attach the sample to the test board. If the board assembly is to be performed at a later time then the samples, at the user discretion, can be baked and vacuum sealed until such time that it is solder attached to the test board or facsimile. The profile used to attach the sample to the test board may be optimized for the soldering operation, but the other two passes must meet the profile requirements of J-STD-020.

NOTE Bumped die devices are commonly soldered to test boards, due to the potential of inflicting handling damage on the loose devices while performing the preconditioning, qualification stresses, and functional testing. If the third reflow pass is used to solder the bumped die devices to boards, care must be taken to minimize damage to the bumped die. If the damage is severe, it could cause devices to fail electrically during the next functional test; if the damage is less severe, it could weaken devices that then fail during reliability stress testing. It may be difficult to determine the root cause for fails if handling damage has occurred.

Since the board attachment replicates a real life process with flux application, reflow and cleaning, steps 4.7 and 4.8 are no longer necessary or mandated prior to submission to reliability stress testing. Flux type shall be documented per section 6.

4.7 Flux application

After the reflow solder cycles are completed, allow the samples to cool at room ambient for 15 minutes minimum. Samples shall then be dipped (full body immersion) in an activated water soluble flux at room ambient for 10 seconds minimum.

Ball Grid Array (BGA), Column Grid Array (CGA) and organic substrate Land Grid Array (LGA) packages do not require flux dipping because their typical board application methods do not use liquid fluxes. Steps 4.8 and 4.9 are not required when flux dipping is omitted for these package types.

The flux application, steps 4.8 and 4.9, is to be omitted for any SMD that has flux or washing limitation as stated as part of its PSL rating (per J-STD-075).

4.8 Cleaning

Clean samples using multiple agitated deionized water rinses. No waiting time is required between flux application and cleaning. Ensure all flux residuals are completely removed.

4.9 Drying

Samples should be dried at room ambient prior to submission to reliability testing.

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4.10 Final electrical test

Submit the samples to electrical and/or functional testing per the room temperature data sheet specification. For the semiconductor manufacturer, this step is optional and may be omitted since it is a supplier's risk. Any valid failures found at this point due to the preconditioning sequence indicate that the SMD may have been classified in the wrong level (MSL and/or PSL) or something is substandard with the test samples. Failure analysis should be conducted. If appropriate, this SMD type should be reevaluated to determine the correct moisture and/or process sensitivity level. This would require resubmitting a sample to a new preconditioning sequence that has been appropriately modified prior to reliability testing per 5.

5 Applicable reliability tests

SMDs should be subjected to the appropriate preconditioning sequence of this document prior to being submitted to reliability tests per JESD47 or the semiconductor manufacturer's in-house reliability procedures.

6 Summary

The following details shall be specified in the applicable procurement document.

a) Revision of J-STD-020 used for the reflow profile.

b) Soak conditions if other than the standard conditions/durations stated in J-STD-020.

c) Number of reflow cycles if other than three.

d) Type of flux if other than Step 4.7.

e) Reliability tests if other than 5.

f) Test conditions and duration of reliability tests in 5.

g) Electrical test description, including test temperature(s).

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Annex A Typical Preconditioning Sequence Flow

Step	Item	Details	Section
1	Initial Electrical Test	- Replace any failing samples - Optional for testing by Supplier	4.1
2	Visual Inspection	- Replace any failing samples - Optional for testing by Supplier	4.2
3	Temperature Cycling	- 5 cycles -40 °C to 60 °C - Optional shipping simulation based on product requirements	4.3
4	Bake	- 24 h at 125 °C - Optional for testing by Supplier	4.4
5	Moisture Soak	- Soak time and conditions per J-STD-020 based on the MSL level	4.5
6	Reflow	- 3 reflow cycles using profiles per J-STD-020, document revision of J-STD-020 used - SnPb or Pb-free profile based on SMD end use process	4.6
7	Flux Application	- 10 s full immersion dip in activated water soluble flux - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.7
8	Cleaning	- DI water rinse - Remove all flux residual - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.8
9	Drying	- Room ambient drying - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.9
10	Final Electrical Test	- **If all samples pass then ready for Reliability Testing** - If valid failures are found then either samples may need to be tested to a lower MSL or PSL classification level or something is substandard with the samples and root cause analysis needs to be performed - Optional for testing by Supplier, but recommended	4.10

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Annex B (informative) Differences between JESD22-A113H and JESD22-A113G

The following list briefly describes most of the changes made to entries that appear in this standard, JESD22-A113H, compared to its predecessor, JESD22-A113G (October 2015). If the change to a concept involves any words added or deleted, it is included. Punctuation changes may not be included.

Clause	Description of change
4.5	Clarified scope of note to include bumped die; included the condition of when reflow preheat effectively dries out the device; and allowed alternative soak duration based on absorption data
4.6.1	Added cautionary note regarding the potential for inflicting damage during reflow simulation of bumped die
6	Added new item b) that alternate soak conditions/durations be documented

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☐ Other ____________________

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