JEDEC STANDARD

Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

JESD22-C101F

(Revision of JESD22-C101E, December 2009)

OCTOBER 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD C101F

FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC-DISCHARGE-WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS

Introduction

This standard describes a uniform method for establishing charged device model (CDM) electrostatic discharge (ESD) “withstand” thresholds. The update allows tests to be partitioned across multiple samples.

This revision enables testing to be done to limit cumulative related failures, and also aligns the testing of CDM to HBM in terms of testing flexibility.

TEST METHOD C101F
FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC-DISCHARGE-WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS

(From JEDEC Board Ballot JCB-04-102, JCB-08-60, JCB-09-87, and JCB-13-53 formulated under the cognizance of the JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

1 Scope

All packaged semiconductor components, thin film circuits, surface acoustic wave (SAW) components, opto-electronic components, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these components are to be evaluated according to this standard. The test methods described in this standard may also be used to evaluate components that are shipped as wafers or bare chips. To perform the tests, the components must be assembled into a package similar to that expected in the final application. The package used shall be recorded.

2 Reference document

JESD625, *Requirements for Handling Electrostatic Discharge-Sensitive (ESDS) Devices.*

3 Terms and definitions

Charged device model (CDM): A specified circuit characterizing an ESD event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface.

Electrostatic discharge (ESD): A sudden transfer of electrostatic charge between bodies or surfaces at different electrostatic potentials.

NOTE The terms “discharge”, “pulse”, “ESD event” and “CDM stresses” are equivalent for the purposes of this document.

Field-induced charging: A charging method using electrostatic induction.

4 Circuit schematic for the CDM simulator

4.1 The waveforms produced by the simulator shall meet the specifications of 5.1 through 8.

4.2 A schematic for the CDM test circuit is shown in Figure 1. (Other equivalent circuits are allowed if the generated waveform meets the requirements of 5.1 through 8.) A detachable discharge head (see Figure 1), consisting of the pogo probe, radial resistor, top ground plane, semi-rigid coaxial cable, and the support arm, is used to initiate the discharge. The top ground plane shall be a square conductive plate with edge length of 63.5 mm ± 6.35 mm (2.5 in ± 0.25 in). The discharge path includes a 1 ohm resistive current probe of at least 3 GHz bandwidth for waveform monitoring. The cable from the 1 ohm resistor to the oscilloscope should also have a bandwidth of at least 3 GHz. The thickness of the FR-4 dielectric shall be 0.381 mm ± 0.038 mm (0.015 in ± 0.0015 in). The dielectric constant of the dielectric shall be specified at 4.7(±5%) at 1 MHz. The charging resistor shown in figure 1 shall be nominally 100 MΩ or greater.

Resistor values higher than 100 MΩ may be used, but this may not allow large devices (greater than 25 mm by 25 mm) to fully saturate before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 MΩ, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for discharging large devices. A procedure for this large device delay characterization is given in 6.2.1.

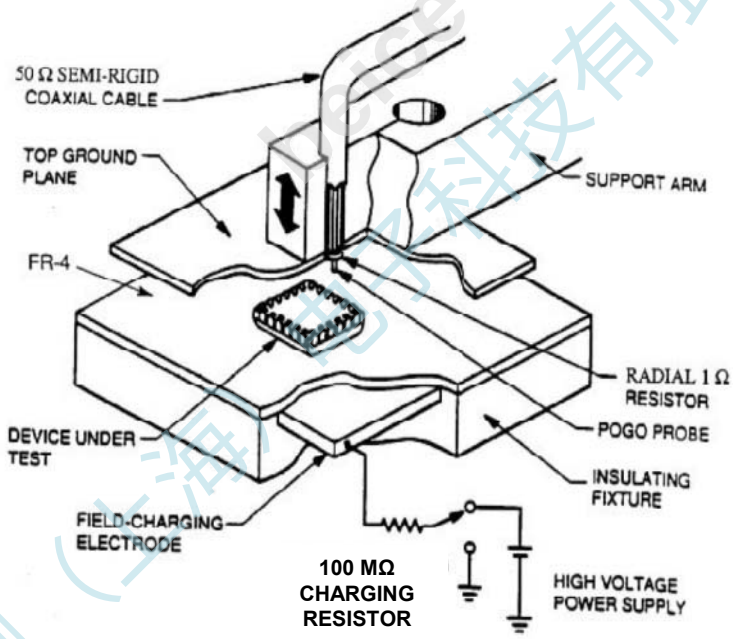

Figure 1 — Field induced CDM simulator

4.3 The Field-Induced Method shall be used to raise the component potential for a subsequent CDM discharge. The component potential is raised by applying the test voltage to the field charging electrode shown in Figure 1. The size of the charging electrode shall be larger than the size of the component and the waveform generated shall meet the requirements in Table 3. The area of the dielectric should be the same as or larger than the charge plate.

5 Measurement instrumentation

5.1 Waveform verification requires the following instrumentation:

a) Oscilloscope with single shot bandwidth of 1 GHz with nominal 50 ohm input impedance and a real time sample rate of 5 gigasamples per second. The bandwidth and sampling rate affect the observed waveform. Use of oscilloscopes with differing bandwidth and sampling rate are permitted only if appropriate hardware or software filtering is used to produce a bandwidth and sampling equivalent to that specified here.

b) Ohmmeter capable of measuring a resistance of 1.0 ± 0.01 ohm.

c) A capacitance meter with a resolution of 0.20 pF, a measurement accuracy of 3% and a measurement frequency of at least 1 MHz.

d) Standard Test modules - One small and one large with the dimensions listed in Table 2.

Table 1 — Test modules

Disk	Small	Large
Diameter mm (inches)	8.89 ± 0.127 (0.350 ± 0.005)	25.4 ± 0.127 (1.000 ± 0.005)
Thickness mm (inches)	1.27 ± 0.05 (0.050 ± 0.002)	1.27 ± 0.05 (0.050 ± 0.002)
Capacitance at 1 MHz	6.8 pF ± 5%	55 pF ± 5%

5.2 The disks shall be made of brass plated with nickel or gold/nickel and may optionally have a gold flash coating over the nickel. They shall be manufactured to the dimensions specified in Table 1 and shall be verified once before the initial use.

NOTE CAUTION shall be exercised during the manufacture of the disks so that they are free from “burrs”. If the perimeter of the disk has “burrs” then arcing may occur altering the results.

5.3 The standard test modules for the CDM simulator can be cleaned in an ultrasonic bath using isopropanol for about 20 seconds and dried in a moderate air stream to prevent charge leakage during test operation.

5.4 The capacitance of the small and large disks shall be measured while sitting on the dielectric/charge plate, and shall conform to the values specified in Table 1.

6 Simulator waveform verification

6.1 The three levels of CDM simulator verification tests are:

– **CDM Equipment** Manufacturer Qualification

– User Verification

– Routine Verification

The tests are described in Table 2.

Table 2 — Waveform verification tests

	Routine Verification	Manufacturer Qualification and User Verification
Record of waveforms required	Yes	Yes
Check (see 7.1)	No	Yes
Tests (see Table 3)	#1	#1, #2, #3, #4

6.2 CDM Equipment Manufacturer Qualification - must be done by the CDM equipment manufacturer when the simulator is installed. High-speed instrumentation must be used, including an oscilloscope that meets the requirements in 5.1. All three qualification tests in clause 8 are required, and the test waveforms must be permanently recorded with copies supplied to the user when requested.

6.2.1 Charging Resistor / Charging Delay Characterization Procedure - Using the large test module disk (see Table 1), measure the average of 10 pulses of the peak current magnitude (Ip) using a +500V plate voltage.

Take one set of measurements with the pre- and post- charge delay setting set to 0 ms. Take another set of measurements with the pre-charge delay set at 500 ms. If the Ip is the same for both measurements, a delay does not need to be added to test large devices. If a delay is needed, 500 ms is long enough for most devices. Alternatively, the tester hardware can be modified by adding a lower valued charging resistor and then re-verified with this procedure. The same procedure can be used on a ground pin of a device to determine the optimum amount of delay needed for a specific device.

6.3 User Verification - done during initial acceptance testing, whenever the equipment is serviced, and on a regular basis at least once per month. The same tests are done as in the manufacturer's qualification. Waveforms must be recorded and stored for comparison with the manufacturer's waveforms and the weekly verification waveforms.

6.4 Routine Verification - Performed at the beginning of each shift the simulator is used. Only test #1 in clause 8 is required. The user shall observe the waveforms and compare them with the previously recorded waveforms.

6.5 If the waveforms do not meet the requirement in clause 8, reject any data obtained after the last successful verification.

7 Measurement procedure

7.1 With the ohmmeter, verify that the resistance of the current sensing resistors in all discharge heads to be used is 1 +/- 0.1 ohm and record the value for use in computing the peak current.

7.2 With the capacitance meter, verify that the capacitance (at 1 MHz) of the small and large disks when placed on the dielectric/charge plate meet the requirements in Table 1.

7.3 With the use of the standard modules in 5.1, perform the four tests in clause 8. For each test,

1) Raise the potential of the standard test module to the voltage indicated in Table 3.

2) Discharge the standard test module at least three times at both positive and negative polarities.

NOTE With the Field-Induced CDM technique, both discharge polarities are obtained on alternate discharges with a single power supply setting. Therefore the power supply voltage may be set to either polarity. The peak currents should have the same magnitude but opposite sign for the two discharge polarities.

3) Record the waveforms using the oscilloscope and take the average values of the parameters specified in Table 3.

4) Repeat the step 1 through step 3 for additional discharge heads as needed.

5) If the waveform characteristics do not meet the requirements in Table 3, clean the test modules (see 6.3) and repeat step 1 through step 3.

6) If the waveform still can not meet the requirements in Table 3, any data obtained since the last verification shall be invalidated and the simulator shall be serviced.

8 Waveform characteristics

The waveforms shall appear as shown in Figure 2 for the positive polarity and its reverse for the negative polarity. The average values specified in 7.3 shall meet the specifications in Table 3.

Table 3 — CDM waveform characteristics

		Test Number			
		#1	#2	#3	#4
Standard test module		**Small**	**Small**	**Large**	**Large**
Test voltage (V)		500 (± 5%)	1000 (± 5%)	200 (± 5%)	500 (± 5%)
Peak current magnitude (A)	Ip	5.75 (± 15%)	11.5 (± 15%)	4.5 (± 15%)	11.5 (± 15%)
Rise time (ps)	tr	<400	<400	-	-
Full width at half height (ns)	Td	1.0 ± 0.5	1.0 ± 0.5	-	-
Undershoot (A, max.)	U-	<50% Ip	<50% Ip	<50% Ip	<50% Ip
Overshoot	U+	<25% Ip	<25% Ip	<25% Ip	<25% Ip

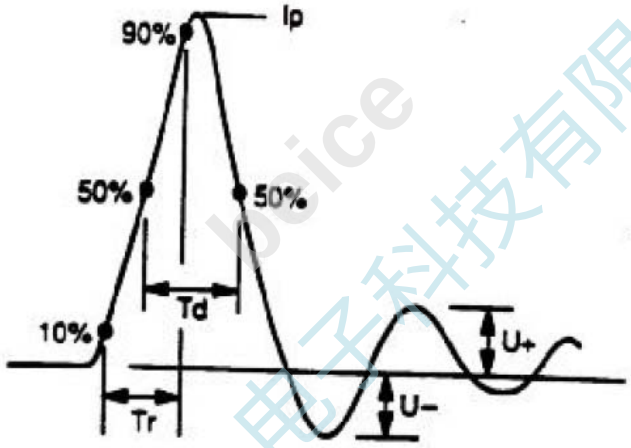

Figure 2 — CDM current waveform

9 Voltage levels

9.1 The recommended voltage levels for CDM ESD testing are:

125 V 500 V
250 V 1000 V

Testing above 1000 volts is not recommended.

NOTE Recommended voltage levels from previous revisions of this standard may also be used (100 V, 200 V, 500 V and 1000 V).

9.2 To determine the threshold more accurately, it is permitted to test at any voltage level >= 100 V and <=1000 V in addition to those recommended above.

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(Revision of Test Method C101E)

10 Test procedures

10.1 The test shall be carried out at room temperature. Ambient humidity shall not exceed 60% RH.

10.2 Testing may begin at any convenient voltage level listed in 9.1.

10.3 Unless otherwise specified, obtain three samples that have been verified to meet their data specifications. For component qualification sample size see JESD47.

10.4 For each component, apply at least one positive and at least one negative discharge to each pin (For Field Induced CDM simulators, a negative pulse automatically follows a positive pulse or vice-versa). Allow enough time (>200 ms) between discharges for the component to reach the full test voltage level. Verify a discharge pulse occurs for each polarity by monitoring the discharge event detector output or connecting an oscilloscope to the current monitoring resistor.

NOTE If there are concerns about the repeatability of current pulses, it is recommended to monitor and record the peak current with an oscilloscope that meets or exceeds the requirements in 5.1.

Stresses may be partitioned by polarity, using a sample size of at least three units per polarity. Pins may also be partitioned into one or more sets of samples, provided that each pin of the device is a member of at least one set. Each set should have a minimum of three units.

Different devices may be used for each polarity as long as at least three devices are used for each polarity; i.e., 3 units for positive discharge and 3 units for negative discharge. Separate devices may also be used for different pin groups as long as each group is tested on 3 devices.

10.5 Test each of the components, using the failure criteria in 11.

10.6 Components that pass the test may be reused at other voltage levels. Components that fail may not be used in tests at other levels. It is permitted to use new components for every voltage level. That is, step-stressing is not required.

10.7 The component passes a voltage level if all three samples stressed at this level pass. The component code fails at the voltage level if one or more samples fail at this level.

10.8 The CDM WITHSTAND THRESHOLD of the COMPONENT is the highest level for which the specified number of stressed samples (usually three out of three) pass. If the component does not pass any level, its threshold is 0 V. In addition, no sample failure shall occur at any test voltage level lower than the withstand threshold.

10.9 CDM stressing and reporting of products shipped and assembled onto printed wiring boards as bare die: Standardized CDM stressing of bare die is currently not defined due to equipment limitations. Products shipped as bare die shall be placed in a package for purposes of performing CDM stressing, as determined by package test limitations. CDM pass/fail voltages shall be reported with the package type(s) used for CDM testing clearly noted. If more than one package type is used for CDM stressing, either all package type data, or worst case data shall be reported.

11 Failure criteria

A component will be defined as a failure if, after exposure to ESD, it no longer meets its data sheet specifications.

NOTE 1 It is suggested that electrical testing be performed within 96 hours of ESD testing. Parametric and functional testing shall be performed at room temperature and, if applicable, at high temperature.

NOTE 2 A failure at a given voltage level may be discounted if proven by failure analysis that is not CDM–ESD related. If the failure analysis is inconclusive a second tightened sample of six devices shall be pulled and stressed at the same voltage level. If no CDM-related failures are observed among these six devices then the part is considered to have passed at that level and the device may be tested at the next voltage level in the stressing regimen.

12 Classification criteria

All samples must meet the test requirements of this document up to a particular voltage level in order for the part to be classified as meeting a particular sensitivity classification.

Devices shall be classified as follows:

CLASS C0A	<125 V
CLASS C0B	125 to <250 V
CLASS C1	250 to <500 V
CLASS C2	500 to <1000 V
CLASS C3	1000 V or greater

13 Supplementary information

13.1 Components used for CDM test shall not be used for any prior or future qualification tests.

13.2 All operators shall wear grounding straps when handling the components. The test components shall be handled with extreme care, using ESD preventive procedure outlined in JESD625**.**

13.3 Components should not be placed within 610 mm (24 inches) of the discharge head while the tester is operating to avoid potential damage from the radiated transient signal.

13.4 Components shall be transported in appropriate ESD-protective packaging. If the CDM withstand threshold is 200 V or less, shipping tubes or tape-and-reel packaging should not be used. Contact customers for information on special packing materials.

Annex A (informative) Differences between JESD22-C101F and JESD22-C101E

This annex briefly describes most of the changes made to entries that appear in this standard, JESD22-C101F, compared to its predecessor, JESD22-C101E (December 2009) as well as changes between earlier revisions. Some punctuation changes are not included.

Clause	Description of Change
4.2	Specified the charging resistor to be nominally 100 MΩ. Added a paragraph related to the charging resistor.
6.2.1	Added a section related to charging resistor characterization. Measurements may be made on a large verification module or packaged IC.
9.1	Modified the recommended stress voltage levels to align with Industry Council recommendations. Limited CDM stress to 1000V or less.
12	Updated Classification levels to align to the Industry Council recommendations and better overall alignment to JS-001.

A.1 Changes to revision of JESD22-C101D (JESD22-C101E)

Clause	Description of Change
10.4	replaced 1st paragraph with new paragraph and note.

A.2 Changes to revision of JESD22-C101C (JESD22-C101D)

Clause	Description of Change
10.4	Modified and added text

A.3 Changes to revision of JESD22-C101B.01 (JESD22-C101C)

Clause	Description of Change
5.1a	Waveform capture bandwidth limited to 1GHz. Higher bandwidth equipment may be used if filtered to produce effective 1GHz. Removed note.
7.1	Require use of actual monitoring resistor value rather than default 1 ohm. Added material at end of sentence.
7.3	Changed number of pulses required for waveform verification from five to three to be consistent with previous change in number of stressing pulses from five to three.
10	Added 10.9 to clarify language describing CDM characterization of die intended to be shipped unpackaged. Such device must be evaluated using suitable package.
11	Clarified treatment of non-CDM test failures
ALL	Corrected typographical and grammatical errors in several sections.

A.4 Changes to revision of JESD22-C101-B (JESD22-C101B.01)

Clause	Description of Change
4.2	Corrected decimal point in the thickness of the FR-4.
Table 2	Clarified clause references in the first column
8	First paragraph, changed 7.2 to 7.3

A.5 Changes to revision of JESD22-C101-A (JESD22-C101-B)

Clause	Description of Change
ALL	Renumbered clauses, due to format issue. (All clauses and subclauses affected.)
3	Added NOTE to Electrostatic Discharge (ESD)
10.4	Changed ‘five’ to ‘three’ 2 times.

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