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IC Latch-Up Test

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IC LATCH-UP TEST

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IC LATCH-UP TEST

(From JEDEC Board Ballots JCB-16-08, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This standard covers the I-test and V_{supply} overvoltage latch-up testing of integrated circuits.

The purpose of this standard is to establish a method for determining IC latch-up characteristics and to define latch-up detection criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up. This test method is applicable to NMOS, CMOS, bipolar, and all variations and combinations of these technologies.

NOTE As these technologies have evolved, it has been necessary to adjust this document to the realities of characterization with limits not imagined when the first latch-up document was generated some 25 years ago. Though it would be simpler to make the original limits of 1.5 times the maximum pin operating voltage an absolute level of goodness, the possibilities of success at this level are limited by the very low voltage technologies, and the medium and high voltage CMOS, BiCMOS and Bipolar technologies (>12 V). The concept of maximum stress voltage (MSV) allows the supplier to characterize latch-up in a way that differentiates between latch-up and EOS. This revision will make it more transparent to the end user that given the limits of certain technologies the subsequent latch-up characterizations are valid.

1.1 Classification

There are two classes for latch-up testing.

- Class I is for testing at room temperature ambient.
- Class II is for testing at the maximum operating ambient temperature (T_a) or maximum operating case temperature (T_c) or maximum operating junction temperature (T_j) in the data sheet.

For Class II testing at the maximum operating T_a or T_c, the ambient temperature or case temperature (T_c) shall be established at the required test value. For Class II testing at the maximum operating T_j, the ambient temperature T_a or the case temperature T_c should be selected to achieve a temperature characteristic of the junction temperature for a given device operating mode(s) during latch-up testing. The maximum operating ambient or case temperature during stress may be calculated based on the methods detailed in Annex B. The values used in Class II testing shall be recorded in the final report.

NOTE Elevated temperature will reduce latch-up resistance, and class II testing is recommended for devices that are required to operate at elevated temperature.

1.2 Latch-up immunity characterization

Product latch-up immunity is characterized by an I/O current injection value and V_{supply} overvoltage value that does not result in a latch-up as defined in this test method. Refer to Table 1 for the recommended range of current and voltage stress, and Table 2 footnotes b, c, and d for the clamping conditions. The actual achieved force current or voltage levels may be reported as mentioned in Annex C.

Table 1 — Latch-up immunity levels

Immunity Level	Test	Magnitude of Trigger Force Current or Voltage
A	Positive I-Test	≥ 100 mA[a]
	Negative I-Test	≥ 100 mA[a]
	Overvoltage Test	1.5 x VDD or MSV, whichever is less[b]
B	If immunity level A cannot be achieved	

[a] The actual injected current may be less than 100mA if pin voltage clamping limits are reached (See Table 2). If Latch-up does not occur in such a condition, then this constitutes a passing test with Immunity Level A. Otherwise, it is classified with Immunity Level B.

[b] The actual applied voltage may be less than 1.5 x VDD or MSV if V_{supply} current clamping limits are reached (See Table 2). If Latch-up does not occur in such a condition, then this constitutes a passing test with Immunity Level A. Otherwise, it is classified with Immunity Level B.

2 Terms and definitions

The following terms and definitions apply to this test method.

cool-down time: The period of time between successive applications of trigger pulses, or the period of time between the removal of the V_{supply} voltage and the application of the next trigger pulse. (See Figure 2, Figure 3, Figure 6, and Table 3.)

DUT: The device under test.

dynamic devices: Devices requiring clocking in order to guarantee a stable state while being tested.

GND (Ground): The common or zero-potential pin(s) of the DUT.

NOTE 1 Ground pins are not latch-up tested. NOTE 2 A ground pin is sometimes called V_{ss}.

input pins: All address, data-in control, V_{ref}, and similar pins.

I/O (bidirectional) pins: Device pins that can be made to operate as an input or an output or in a high-impedance state.

2 Terms and definitions (cont'd)

Isupply: The total supply current in each V_{supply} pin (or pin group) with the DUT biased as indicated in Table 2.

I-test: A latch-up test that supplies positive and negative current pulses to the pin under test.

latch-up: A state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition.

NOTE 1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative.

NOTE 2 Latch-up will not damage the device provided that the current through the low-impedance path is sufficiently limited in magnitude or duration.

logic-high: A level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states.

NOTE 1 For digital devices, the maximum value of the high logic level voltage is used for latch-up testing. The maximum logic high level is designated as V_{max}.

NOTE 2 For non-digital devices, the maximum operating voltage that can be applied to that pin as defined in the device specification is used for latch-up testing.

logic-low: A level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states.

NOTE 1 For digital devices, the minimum value of the low logic level voltage is used for latch-up testing. The minimum logic low level is designated as V_{min}.

NOTE 2 For non-digital devices, the minimum operating voltage that can be applied to that pin as defined in the device specification is used for latch-up testing.

maximum V_{supply}; maximum operating voltage: The maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification.

NOTE 1 **"**Maximum" refers to the magnitude of supply voltage and can be either positive or negative.

NOTE 2 The maximum voltage is ***not the absolute maximum rated voltage, i.e., the voltage beyond which permanent damage is likely.***

2 Terms and definitions (cont'd)

maximum stress voltage (MSV): The maximum voltage allowed to be placed on any given pin during latch-up immunity testing without causing irreversible damage to the device from a catastrophic breakdown of the silicon device or circuit not related to latch-up.

NOTE 1 A positive MSV is higher than the maximum operating voltage and a negative MSV is lower than the minimum operating voltage.

NOTE 2 MSV is NOT the same as the absolute maximum voltage rating (AMR) from the device data sheet. MSV applies to latch-up testing only, protecting the DUT from physical damage from stress mechanisms not directly related to latch-up. An example of an unrelated stress is one exceeding the destructive breakdown voltage of a pin resulting in non-latch-up induced catastrophic breakdown of the silicon device / circuit. MSV may be different for each pin and each polarity during testing, depending on process technology and circuit topology. In many medium and high voltage designs (>12 V), MSV may be nearly the same value as AMR. Further, the MSV value depends on the pulse width used during latch-up testing. Shorter pulse widths may allow a higher value for MSV. Therefore, the MSV value chosen should take into account the pulse width as well as process technology and circuit topology.

"no connect" pin: A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device.

NOTE All "no connect" pins shall be left in an open (floating) state during latch-up testing.

nominal I_{supply} (I_{nom}): The measured dc supply current for each V_{supply} pin (or pin group) with the DUT biased at the test temperature as defined in clause 4 and Table 2.

output pin: A device pin that generates a signal or voltage level as a normal function during the normal operation of the device.

NOTE Output pins, though left in an open (floating) state during testing of other pin types, are latch-up tested.

power supply: A component in the test system that supplies voltage and current to the DUT.

preconditioned pin: A device pin that has been placed in a defined state or condition (input, output, high impedance, etc.) by applying control vectors to the DUT.

test condition: The test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages, and preconditioning vectors applied to the DUT during the latch-up test.

timing-related input pin: A pin such as clock crystal oscillator, charge pump circuit, etc., required to place the DUT in a normal operating mode.

NOTE Required timing signals may be applied by the latch-up tester, external equipment, and/or external components as appropriate.

trigger pulse: The positive or negative current pulse (I-Test) or voltage pulse (V_{supply} overvoltage test) applied to any pin under test in an attempt to induce latch-up (see Figure 2, Figure 3 and Figure 6).

2 Terms and definitions (cont'd)

trigger duration: The duration of an applied pulse from the trigger source. (See Figure 2, Figure 3, Figure 6 and Table 3.)

V_{supply} pin (or pin group): A supply pin is any pin that provides current to a circuit. Supply pins typically transmit no information (such as digital or analog signals, timing, clock signals, voltage or current reference levels). For the purpose of latch-up testing, power pins are treated as supply pins.

NOTE 1 Generally, it is permissible to treat equal-potential voltage source pins as one V_{supply} pin (or pin group) and connect them to one power supply.

NOTE 2 When forming V_{supply} pins (or pin groups), the combination of V_{supply} pins with significantly different supply current levels is not recommended as this would make it difficult to detect significant current changes on low supply current pins.

V_{supply} overvoltage test: A latch-up test that supplies overvoltage pulses to the V_{supply} pin (or pin group) under test.

3 Apparatus and material

The apparatus required for this test method includes the following:

3.1 Latch-up tester

Test equipment capable of performing the tests as specified in this document. For devices requiring dynamic testing, the test equipment shall be capable of supplying timing signals and logic setup vectors required to control the I/O pin output states as specified in 4.2.3. The required timing signals and logic vectors may be applied by the latch-up tester itself, external equipment, and/or external components as appropriate.

3.2 Automated test equipment (ATE)

A device tester capable of performing full functional and parametric testing of the device to the device specification requirements.

3.3 Heat source

Equipment capable of heating and maintaining the DUT at the maximum operating temperature specified in the device specification during the latch-up test.

4 Procedure

4.1 General latch-up test procedure

Prior to the latch-up test, the device needs to be in a stable state with reproducible I_{nom}. Engineering judgment may be needed to achieve sufficient stability. The supply current should be made as low as practicable. The supply current must be stable enough and low enough to reliably detect the supply current increase if latch-up occurs.

A minimum of three (3) devices shall be subjected to latch-up testing using the I-test and supply overvoltage test. It is allowed to partition I-test, supply overvoltage test, or test combinations by using at least 3 fresh devices for each partition. All devices to be latch-up tested must have passed ATE testing to the device specification requirements. Before latch-up testing, the device continuity in the socket should be checked to avoid false latch-up failures. The latch-up test flow shall be as shown in Figure 1. The devices to be tested shall be subjected to the test conditions specified in Table 2 and Table 3. All "no connect" pins on the DUT shall be left open (floating) at all times.

All pins on the DUT, with the exception of "no connect" pins and timing related pins, shall be latch-up tested. The Input, output, and configurable I/O pins are to be tested with the I-test and the V_{supply} pins tested with the Overvoltage test. This includes special pins defined in Annex A. The passing current or voltage values for the special pins can be used for determining the values of the passive-components connected to the pins. I/O pins shall be tested in all possible operating states or the worst case operating state (typically high impedance for configurable I/O pins). Dynamic devices shall be tested per 4.2.3. When a device is sufficiently complex that testing of all configurable I/O pins in the worst case condition is not practicable, the device should be conditioned with a set of vectors representative of the typical operation of the device as determined by engineering judgment. When an I/O pin cannot be tested in the high impedance state, the I/O shall be tested in a valid logic state. Untested pins and pins that could not be completely tested shall be recorded as specified in 4.2.5 and the user shall be informed of all I/O pins that were not tested or tested in all states. After latch-up testing, all devices must pass the criteria specified in Section 5.

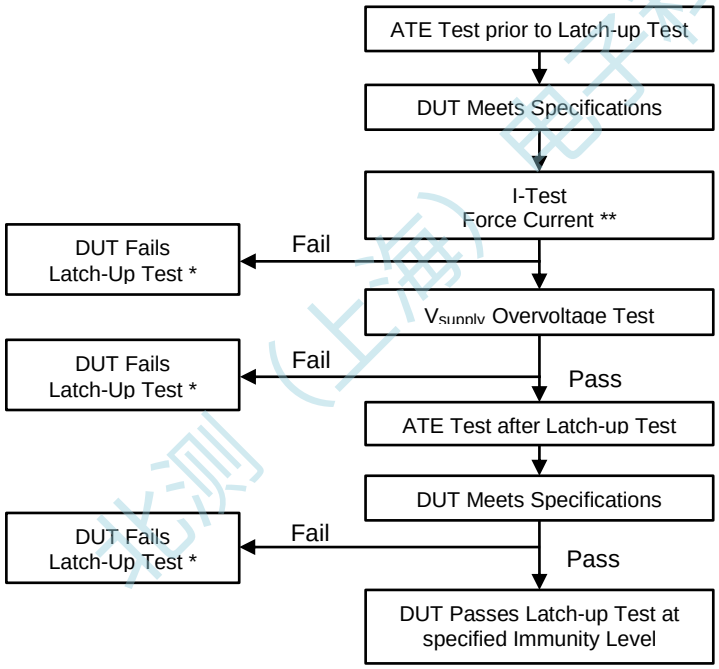


Figure 1 — Typical latch-up test flow

4.1 General latch-up test procedure (cont'd)

Table 2 — Test matrix[7]

Test type	Trigger polarity	Condition of untested input pins	Test temperature classification	V_{supply} conditions	Trigger test conditions for pin or supply group under test	Latch-up detection criteria[5, 6]
I-Test	POSITIVE see Figure 4	Max Logic High[1]	Temperature Class I Room Temperature Temperature Class II Maximum ambient operating temperature	Maximum operating voltage for each V_{supply} pin group per device specification	See Table 1 for stress current range and Note 3 for clamp voltage	If absolute I_{nom} is $\leq$ 25 mA, then absolute I_{nom} + 10 mA is used Or If absolute I_{nom} is > 25 mA, then > 1.4 X absolute I_{nom} is used
		Min Logic Low[1]				
	NEGATIVE see Figure 5	Max Logic High[1]			See Table 1 for stress current range and Note 4 for clamp voltage	
		Min Logic Low[1]				
V_{supply} Overvoltage test	See Figure 7	Max Logic High[1]			See Table 1 for stress voltage and Note 2 for clamp current	
		Min Logic Low[1]				

NOTE 1 Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to non-digital device it means the maximum high or minimum low voltage the can be supplied to the pin per the device specification.

NOTE 2 During supply overvoltage latch-up tests, it is common to combine several IC supply pins of the same voltage into one supply group. It is necessary to combine supply pins into one group if they are connected internally. The current clamp for the supply group is set according to the total nominal supply current of the group. The clamp current for the j^{th} supply group is the greater of: a. or b.

a. $I_{clamp\,j} = 100\ mA + I_{nom\,j} = 100\ mA + \sum_{\text{All supplies in supply group j}} I_{nom\,i}$

b. $I_{clamp\,j} = 1.5 \times I_{nom\,j} = 1.5 \times \sum_{\text{all supplies in supply group j}} I_{nom\,i}$

NOTE 3 The pin clamping voltage for positive I-test is giving by $V_{clamp} = V_{max} + 0.5x(V_{max} - V_{min})$ with an upper limit of $1.5xV_{max}$, where V_{max} (logic high) and V_{min} (logic low) are defined in Section 2. If the Maximum Stress Voltage (MSV) for the pin (See Section 2) is less than $V_{max} + 0.5x(V_{max} - V_{min})$ or $1.5xV_{max}$, then the pin clamping voltage is given by V_{clamp} = MSV. In some instances the forcing current required and the voltage limit may have opposite polarities. Two- quadrant power supplies are not capable of providing positive injection current with negative clamping voltage. Four-quadrant power supplies do not share this limitation.

NOTE 4 The pin clamping voltage for negative I-test is given by $V_{clamp} = V_{min} - 0.5x(V_{max} - V_{min})$ with a lower limit of $-0.5xV_{max}$, where V_{max} (logic high) and V_{min} (logic low) are defined in Section 2. If the Maximum Stress Voltage (MSV) for the pin is greater than $V_{min} - 0.5x(V_{max} - V_{min})$ or $-0.5xV_{max}$, then the pin clamping voltage is given by V_{clamp} = MSV. In some instances the forcing current required and the voltage limit may have opposite polarities. Two- quadrant power supplies are not capable of providing negative injection current with positive clamping voltage. Four-quadrant power supplies do not share this limitation.

NOTE 5 If the trigger test condition reaches the voltage of current clamp limit and latch-up has not occurred, the pin passes the latch-up test. See clause 5 for the complete failure definition.

NOTE 6 During I-test or supply overvoltage test, the supply currents for all supply groups are monitored for latch-up occurrence. Failure occurs if any supply current exceeds the limit in Table 2.

NOTE 7 The trigger conditions herein are not indicative of appropriate trigger conditions for all devices. Appropriate trigger conditions may be more or less stringent. When trigger conditions used in testing differ from this table, the trigger conditions used must be defined in the test results.

4.2 Detailed latch-up test procedure

4.2.1 I-test

The I-test shall be performed as follows:

1) The devices shall be subjected to the I-test as indicated in Figure 1/Table 2 and Figure 2 and Figure 3/Table 3.

2) Bias the DUT as indicated in Figure 4. All input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins, shall be tied to the maximum logic-high level specified in the device specification. Input pins used for preconditioning must be tested in their defined state (pins that are tied to a logic-high level to precondition the DUT can only be tested in the logic-high state; pins that are tied to a logic-low level to precondition the DUT can only be tested in the logic-low state). Allow the DUT to stabilize at the test temperature.

3) Put the pin under test in logic-high state. Measure nominal I_{supply} (I_{nom}) for each V_{supply} pin (or pin group, see Table 2). Then, apply the positive current trigger (per Table 2 for a duration as specified in Table 3) to the pin under test.

4) After the trigger source has been removed, return the pin under test to the level it was in before the application of the trigger pulse, and measure the I_{supply} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in Table 2, latch-up has occurred and power must be removed from the DUT. If latch-up has occurred, stop the test; the DUT has failed latch-up testing. Using a new part, return to step 1 and continue testing.

5) If latch-up has not occurred, after the necessary cool-down time (see Table 3), repeat steps 3 and 4 for all pins to be tested (noting the exceptions stated in step 2).

6) Repeat steps 2 through 5 with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins tied to the minimum logic-low level specified in the device specification.

7) Bias the DUT as indicated in Figure 5 with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins shall be tied to the maximum logic-high level specified in the device specification (noting the exceptions stated in step 2).

8) Put the pin under test in logic-low state. Measure nominal I_{supply} (I_{nom}) for each V_{supply} pin (or pin group, see Table 2). Then, apply the negative current trigger source below ground (per Table 2 for a duration as specified in Table 3) to the pin under test.

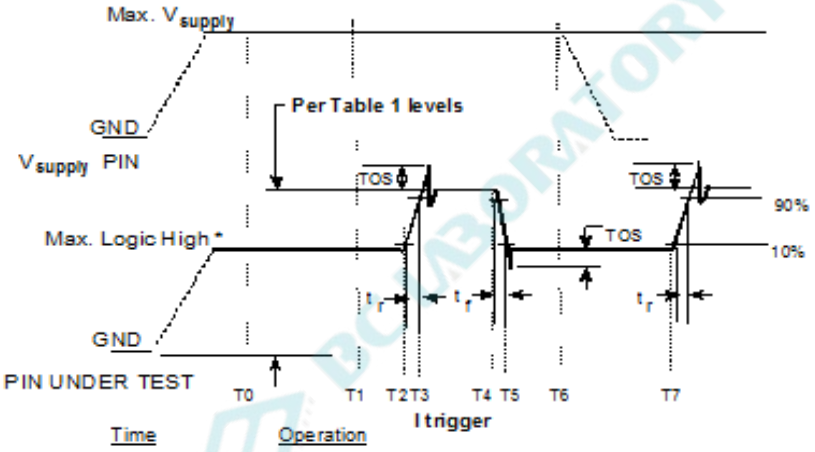
9) After the trigger source has been removed, return the pin under test to the level it was in before the application of the trigger pulse and measure the I_{supply} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in Table 2, latch-up has occurred and power must be removed from the DUT. If latch-up has occurred, stop the test; the DUT has failed latch-up testing. Using a new part, return to step 1 and continue testing.

10) If latch-up has not occurred, after the necessary cool-down time (see Table 3), repeat steps 8 and 9 for all pins to be tested.

11) Repeat steps 8 through 10 with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins tied to the minimum logic-low level specified in the device specification (noting the exceptions stated in step 2).

I-test in 4.2.1 does not require the removal of power-supply voltage between stresses, i.e., cool-down time. Users should evaluate the risk of leaving the power-supply on.

4.2.1 I-test (cont'd)

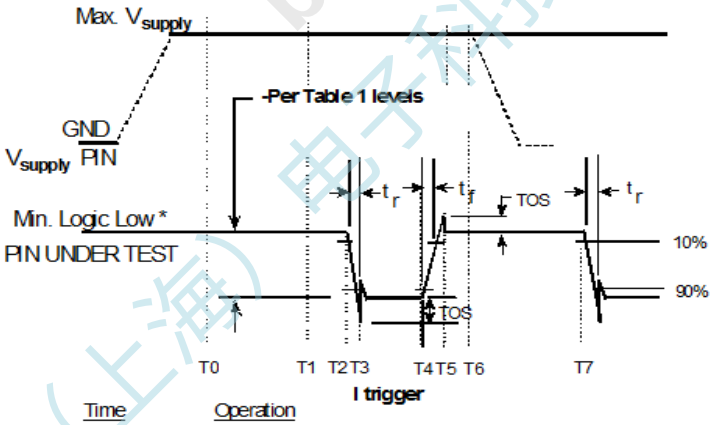


Time	Operation
T0 → T1	Wait time prior to I_{supply} measurement.
T5 → T7	Cool down time (Tcool)
T5 → T6	Wait time prior to I_{supply} measurement.
T6	Measure I_{supply}, If any $I_{supply} \geq$ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from then on.

* Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device.

NOTE The pin under test shall be set to logic high before positive current trigger. It is permissible to start positive current trigger from logic low, but failing results should be confirmed from the logic high state.

Figure 2 — Test waveform for positive I-test



Time	Operation
T0 → T1	Wait time prior to I_{supply} measurement.
T5 → T7	Cool down time (Tcool)
T5 → T6	Wait time prior to I_{supply} measurement.
T6	Measure I_{supply}, If any $I_{supply} \geq$ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from then on.

* Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device.

NOTE The pin under test shall be set to logic low before negative current trigger. It is permissible to start negative current trigger from logic high, but failing results should be confirmed from the logic low state.

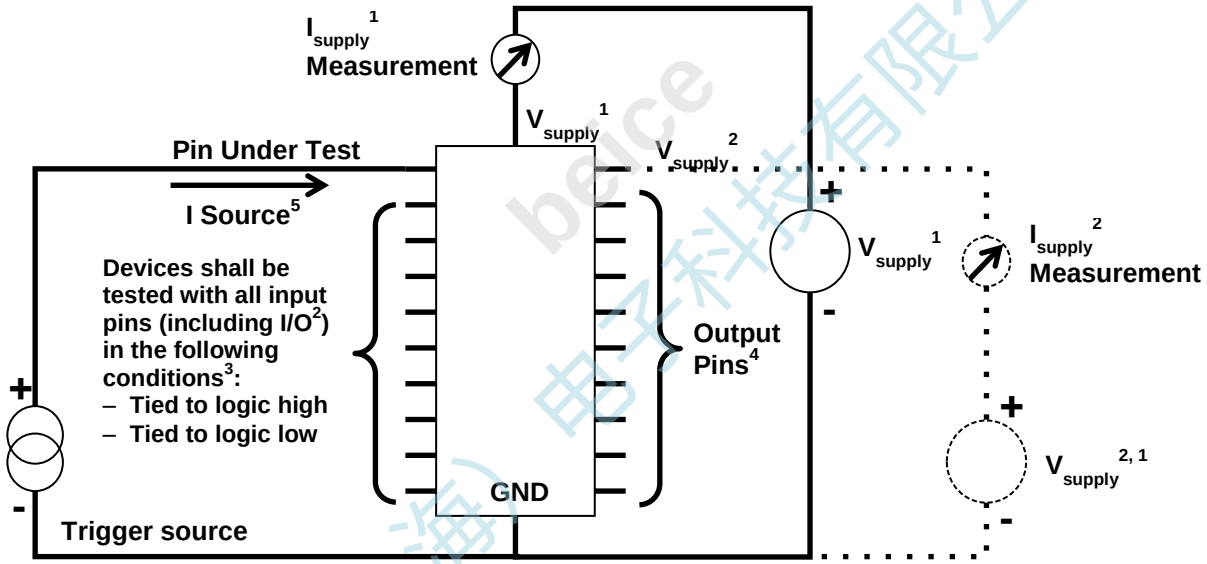
Figure 3 — Test waveform for negative I-test

4.2.1 I-test (cont'd)

Table 3 — Timing specification for I-test

Symbol	Time interval	Parameter	Limits	
			MIN	MAX
$t_{measure}$*	T0 to T1 T5 to T6	Waiting time before measuring I_{supply}	3 ms	5 s
t_r	T2 to T3	Trigger rise time	1 µs**	5 ms
t_{width}	T2 to T4	Trigger duration	$2*t_r$	1 s
t_f	T4 to T5	Trigger fall time	1 µs**	5 ms
t_{cool}	T5 to T7	Cool down time	> = T_{width}	
TOS		Trigger over-shoot	+/- 5% of pulse voltage	

* The wait time shall be sufficient to allow for power supply ramp up/down and stabilization of I_{supply}
** Min trigger rise/fall time reduced from 5 µs to account for ATE testers. Some testers may not be able to measure this parameter, however it can be measured with an oscilloscope



NOTE 1 DUT biasing shall include additional V_{supply} as required.

NOTE 2 DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1. I/O pins in the output state shall be open circuit.

NOTE 3 Logic high and logic low shall be per the device specification. When logic levels are used in respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.

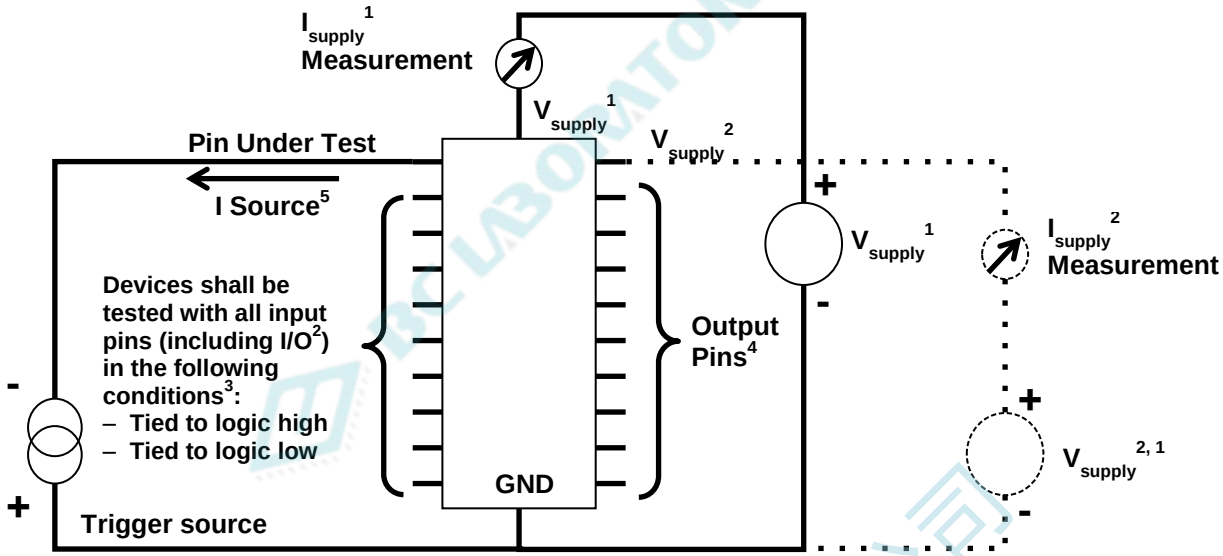
NOTE 4 Output pins shall be open circuit except when latch-up tested.

NOTE 5 The trigger test condition is defined in Figure 2 and Table 2.

NOTE 6 Dynamic devices may have timing signals applied per 4.2.3.

Figure 4 — Equivalent circuit for positive input/output I-test latch-up testing

4.2.1 I-test (cont'd)



NOTE 1 DUT biasing shall include additional V_{supply} as required.

NOTE 2 DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1.

I/O pins in the output state shall be open circuit.

NOTE 3 Logic high and logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification, unless these conditions violate the device setup condition requirements

NOTE 4 Output pins shall be open circuit except when latch-up tested.

NOTE 5 The trigger test condition is defined in Figure 3 and Table 2.

NOTE 6 Dynamic devices may have timing signals applied per 4.2.3.

Figure 5 — Equivalent circuit for negative input/output I test latch-up testing

4.2.1 I-test (cont'd)

4.2.1.1 Supply current limits

This section is applicable to cases where a given supply is reported as passing using the criteria defined in Table 2.

Latch-up test equipment power supplies, used for V_{supply} pins or for biasing I/O pins, generally have current limits (I_{limit}) assigned for device EOS and test fixture protection considerations. When a supply current or I/O biasing current reaches these power supply limits, the latch-up test result may be invalid.

A latch-up event that reaches the I_{limit} could also collapse the V_{supply} below the latch-up holding voltage and terminate latch-up before the automated test equipment detects it as a latch-up failure. The stability of all the tester supplies that measure currents should be monitored during latch-up testing to ensure that the currents are kept below the assigned I_{limit}. This includes tester supplies used for biasing I/O pins at logic-high or logic-low states or for preconditioning of I/O pins, for instance.

General test procedures and recommendations:

- All tester supply voltages should remain within their specified range, including the time before, after, and while the current trigger is applied. It is recommended that for each V_{supply} pin (or pin group), the I_{limit} is initially set to at least:
  - I_{nom} plus two times the injection current, or
  - 1.4 times I_{nom}, whichever is higher.
- If the voltage of any tester supply collapses or reaches its I_{limit} while the trigger source is applied to the pin, the I-test becomes invalid and needs to be repeated with a higher I_{limit} setting.

It is permissible to provide any I-test characterization results obtained with lower I_{limit} settings in the latch-up report. These characterization results can be provided in addition to the required absolute I-test passing levels with stable tester supplies (see examples in Annex C). Reported entries should include the specific I_{limit} settings used and the corresponding collapsing power supplies during the current trigger. These additional characterization data may appropriately reflect latch-up robustness in system applications exhibiting supply current limitations similar to these lower I_{limit} settings.

4.2 Detailed latch-up test procedure (cont'd)

4.2.2 V_{supply} overvoltage test

The V_{supply} overvoltage test shall be performed on each V_{supply} pin (or pin group) as indicated below. To provide a true indication of latch-up for given test conditions input pins configured as logic-high shall remain within the valid logic-high region as defined in the device specification (typically greater than 70% of the V_{supply} overvoltage test level). If input pin levels fall outside of the valid logic-high region, the device may change state causing a change in I_{nom} and invalid test data. If a latch-up failure occurs when the input pin(s) fall outside of the valid logic-high region, engineering judgment must be used to determine whether the failure is a valid latch-up condition or a failure caused by a change in state.

1) The devices shall be subjected to the V_{supply} overvoltage test as indicated in Figure l/Table 2 and Figure 6 and Table 4.

2) Bias the DUT as indicated in Figure 7. All input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins shall be tied to the maximum logic-high level specified in device specification. Input pins used for preconditioning must be tested in their defined state (pins that are tied to a logic-high level to precondition the DUT can only be tested in the logic-high state, pins that are tied to a logic-low level to precondition the DUT can only be tested in the logic-low state). Allow the DUT to stabilize at the test temperature. Measure nominal I_{supply} (I_{nom}) for each V_{supply} pin (or pin group, see Table 2) at this time.

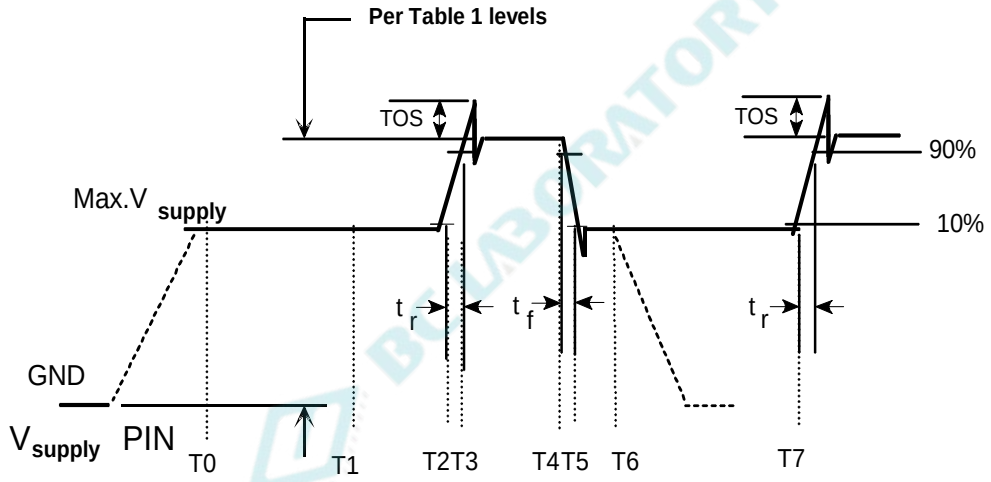
3) Apply the voltage trigger source (per Table 2 for a duration as specified in Table 4) to the V_{supply} pin (or pin group) under test.

4) After the trigger source has been removed, return the V_{supply} pin under test to the state it was in before the application of the trigger pulse and measure the I_{supply} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in Table 2, latch-up has occurred and power must be removed from the DUT. If latch-up has occurred stop the test; the DUT has failed latch-up testing. Using a new part, return to step 1 and continue testing.

5) If latch-up has not occurred, after the necessary cool-down time (see Table 4), repeat steps 2 through 4 with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins tied to the minimum logic-low level specified in the device specification (noting the exceptions stated in step 2).

6) Repeat steps 2 through 5 until each V_{supply} pin (or pin group) has been tested.

4.2.2 V_{supply} overvoltage test (cont'd)



Time	Operation
T0 → T1	Wait time prior to I_{supply} measurement.
T0 → T2,T5 → T7	Cool down time (Tcool)
T5 → T6	Wait time prior to I_{supply} measurement.
T6	Measure I_{supply}, If any $I_{supply} \geq$ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from then on.

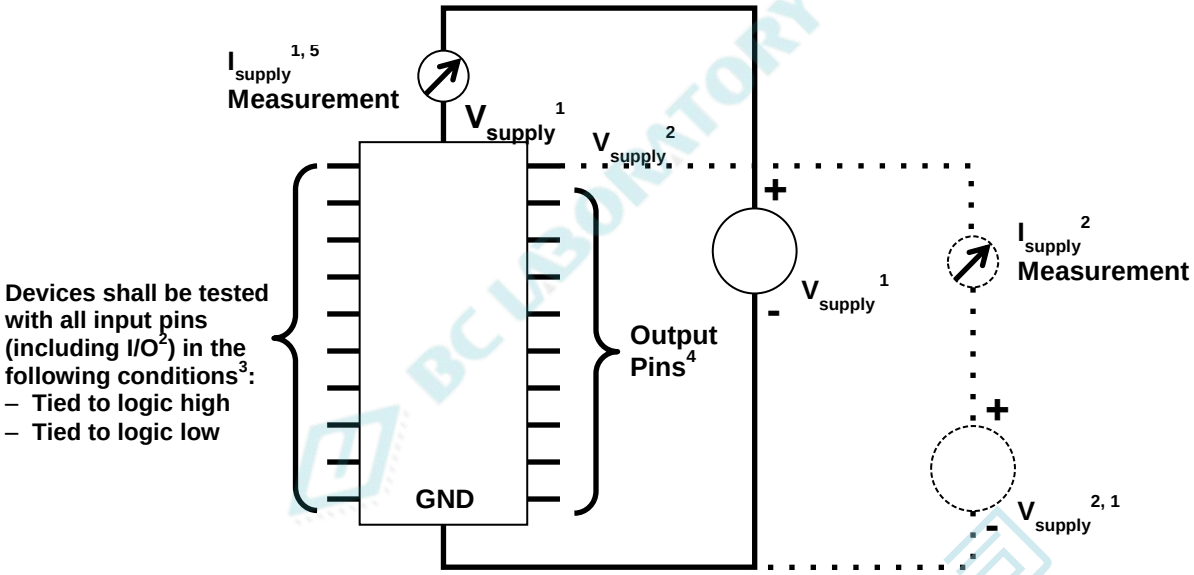
Figure 6 — Test waveform for V_{supply} overvoltage

Table 4 — Timing specification for V_{supply} overvoltage test

Symbol	Time interval	Parameter	Limits	
			MIN	MAX
$t_{measure}$*	T0 to T1 T5 to T6	Waiting time before measuring I_{supply}	3 ms	5 s
t_r	T2 to T3	Trigger rise time	5 µs	100 ms**
t_{width}	T2 to T4	Trigger duration	2*t_r	1 s
t_f	T4 to T5	Trigger fall time	5 µs	100 ms**
t_{cool}	T5 to T7	cool down time	> = T_{width}	
TOS		Trigger over-shoot	+/- 5% of pulse voltage	

* The wait time shall be sufficient to allow for power supply ramp up/down and stabilization of I_{supply}
** Max trigger rise/fall increased from 5ms to allow for high voltage and/or power devices. Some testers may not be able to measure this parameter, however it can be measured with an oscilloscope.

4.2.2 V_{supply} overvoltage test (cont'd)



NOTE 1 DUT biasing shall include additional $V_{supplies}$ as required.
NOTE 2 DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1. I/O pins in the output state shall be open circuit.
NOTE 3 Logic high and logic low shall be per the device specification. When logic levels are used in respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification, unless these conditions violate the device setup condition requirements.
NOTE 4 Output pins shall be open circuit except when latch-up tested.
NOTE 5 The trigger test condition is defined in figure 6 and Table 2.
NOTE 6 Dynamic devices may have timing signals applied per 4.2.3.

Figure 7 — The equivalent circuit for V_{supply} overvoltage test latch-up testing

4.2.3 Testing dynamic devices

Devices that during normal operating conditions have a clock and/or other timing signal inputs may be latch-up tested in a static manner as indicated in 4.2.1 and 4.2.2. If the device does not show a stable I_{supply} (I_{nom}) measurement or appears to latch up, the clock and/or other associated timing and control signals, as defined in the device specification, may be applied to the device during latch-up testing per 4.2.1 and 4.2.2. Unless otherwise specified, the clock pins and other associated timing pins used to place the device in a stable state shall not be latch-up tested while being used to stabilize the device. The supplier shall maintain records indicating how the device was tested, as indicated in 4.2.5.

4.2.4 DUT disposition

Latch-up testing is potentially destructive. Devices used for latch-up testing shall not be used or considered as salable devices.

4.2.5 Record keeping

Suppliers will report:

- The version of JEDEC JESD78 followed during the testing
- Integrated circuit classification per 1.1 and Table 3.
- The MSV value(s) on a pin-by-pin basis if appropriate or if requested for information.
- The I_{limit} settings per V_{supply} pin (or pin group).
- Latch up immunity capability (sustained stress current and voltage) on a device or pin-by-pin basis.

Appropriate data shall be recorded for correlation including the following information in the latch-up characterization in case the test has to be rerun. Example of recorded data may include clock frequency (for dynamic devices), pulse width, vector set used for preconditioning, temperature, trigger condition, supply current limits (I_{limit}), and latch-up I_{supply} current. Recorded data is especially important for failing pins. Also, for pins that would never have detected latch-up on the application should be recorded as special pins per Annex A.

Examples for recording and reporting data are shown in Annex C.

5 Latch-up detection criteria

A device is considered to have experienced latch-up if it meets the latch-up detection criteria listed in Table 2 or it does not pass the device ATE requirement. ATE testing is required to detect damage from short duration latch-up events or EOS that may occur during latch-up stress.

NOTE 1 Comments on ATE testing following latch-up stress:

- Latch-up events triggered during supply overvoltage or current injection tests may damage the device, and the damage could end the latch-up event before the latch-up tester detects the failure (short-duration latch-up). An ATE test failure may be the only indication of this kind of latch-up.

- Latch-up test current injection could directly damage the DUT through EOS without an actual latch-up event. ATE testing can be used to confirm this source of device damage.

- These damage sources (undetected short-duration latch-up events and EOS) may prevent proper control of the device during automated latch-up testing and could invalidate some latch-up test results for some pins on the device.

NOTE 2 ATE failure disposition guidelines:

- If the ATE failure is suspected to be caused by an ESD issue (not latch-up stress), repeat the latch-up test with fresh samples.

- If the ATE failure is suspected to be caused by EOS damage during latch-up stress, adjust the trigger pulse according to Table 3, and repeat the latch-up test with fresh samples.

- If the samples still fail ATE test after the above evaluation the device fails Immunity Level A latch-up. On fresh samples the IO trigger current can be adjusted to a value at which the integrated circuit can pass the latch-up test as well as ATE following latch-up test.

6 Summary

The following details shall be specified in the procurement document, if different from the requirements in this standard:

1) Class (I or II) per this document.

2) Sample size.

3) Trigger test conditions.

4) Latch-up test temperature.

5) Latch-up detection criteria.

6) Pulse/Trigger conditions.

7) Vector set used to precondition the device.

Annex A (informative) Examples of special pins that are connected to passive components

Complex integrated circuits contain a wide variety of pins with special properties that require engineering judgment during latch-up testing. This annex is intended to give guidance when considering the latch-up testing of individual pins that do not fall into the category of digital inputs, outputs or bidirectional pins with ground to power supply voltage swings. All of the pins under discussion are assumed to be non-power supply pins and are therefore subject to the I-test. Some of the pins may have names that suggest that they are power supply pins but in general that is not the case. Many of the pins in question are connected to passive components and it is fair to ask the question, does latch-up testing of this pin make sense at all since they have no direct contact to an external voltage to induce latch-up?

NOTE Annex A should not be used as a way to avoid testing pins but as guidance toward what is reasonable. If a pin can be blindly tested to the stress levels of Table 2 this should be done since it raises the least amount of questions.

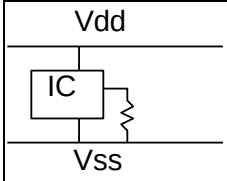
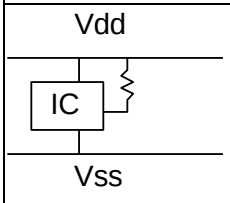
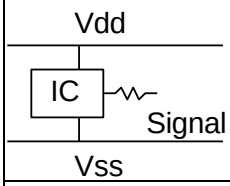
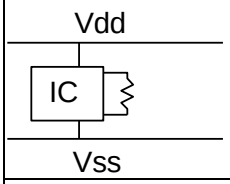
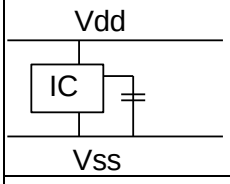
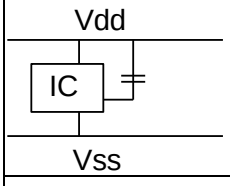
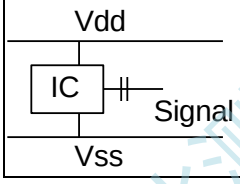
A.1 Passive component pins

Many integrated circuit pins connect to passive components only: resistors, capacitors and inductors. In some instances these components are needed for device stability and it is necessary that the passive components be attached to the device during latch-up testing. Reasonable arguments can be made for the elimination or reduction of stress levels for pins that will see only passive components, or passive components that come between the integrated circuit and active signal lines. These arguments ignore the possibility of latch-up due to transients such as electrostatic discharge (ESD). Since the possibility of latch-up being induced by ESD is a real concern, the elimination of all latch-up testing on a pin should be avoided.

A.2 Digital differential input pins

Digital differential pins create a special case when considering stressing with inputs high and low since the two pins cannot be held high or low simultaneously. The definition of holding all inputs high or low must be modified. For all inputs high the positive input of the differential pin should be held high and the negative input held low. For all inputs low the positive input should be held low and the negative input held high. (Note that the designations positive and negative are purely arbitrary.)

Annex A (informative) Examples of special pins that are connected to passive components (cont'd)

Circuit	Considerations
	A pin in which a resistor goes only to ground has little likelihood of triggering latch-up and could be considered for no test. Only ground bounce could lead to latch-up triggering current. To determine the amount of trigger current determine a likely amount of ground bounce and inject plus and minus current equal to ground bounce voltage divided by the resistor value.
	This is very similar to the situation in which the resistor goes to Vss except that bounce in Vdd could lead to trigger currents. To determine the amount of trigger current determine a likely amount of Vdd bounce and inject plus and minus current equal to Vdd bounce voltage divided by the resistor value. Latch-up sensitivity to Vdd overvoltage should also be tested.
	A resistor between an input signal and an input will reduce the amount of injected current. The injected latch-up current can be reduced to the compliance voltage during latch-up stress divided by the resistor value if this is less than the standard forcing current.
	This resistor attachment shows very little likelihood of causing latch-up and not testing the pins is reasonable.
	Not a likely source of latch-up.
	Not a likely source of latch-up.
	A capacitor will prevent dc current injection but that does not mean that the pin is latch-up free due to voltage transients. If the part is tested without the capacitor the current injection level can be determined by assuming a worst case voltage transient on the signal and calculating the current through the capacitor.

Annex B (informative) Calculation of Operating Ambient or Operating Case Temperature for a Given Operating Junction Temperature

In the following, methods for calculating maximum operating T_a or the maximum operating T_c are provided by using three parameters. The first parameter is $P_{LU,}$ the average power consumption defined as the product of nominal supply voltage and nominal supply current under the latch-up test condition. The second and the third parameters are θ_{ja} and $\theta_{jc,}$ the thermal resistance relative to ambient and package case respectively. The guideline for these parameters is the ones at still air.

a) Calculating operating ambient temperature T_a

If the operating ambient temperature is T_a, the operating junction temperature is T_j, the device power consumption under latch-up test condition is P_{LU}, and the package thermal resistance is θ_{ja}, the following equation is used for calculating T_a from the required T_j:

$$T_a = T_j - P_{LU} * \theta_{ja}$$

b) Calculating operating case temperature T_c

If the operating case temperature is T_c, the operating junction temperature is T_j, the device power consumption under latch-up test condition is P_{LU}, and the package thermal resistance is θ_{jc}, the following equation is used for calculating T_c from the required T_j:

$$T_c = T_j - P_{LU} * \theta_{jc}$$

Annex C (informative) Examples for recording and reporting data

C.1 Examples of recording data

Pin Group	Test Type	Level Passed	$+V_{CLAMP}$(V)	$-V_{CLAMP}$(V)	I_{CLAMP}(mA)	T (˚C)
List of I/Os	Latch-up I-test	Not tested[1]	N/A	N/A	N/A	125
List of I/Os	Latch-up I-test	+50 to 100[2]	$1.5xV_{DDMAX}$[4]			125
List of I/Os	Latch-up I-test	< +50[3]	$1.1xV_{DDMAX}$[5]			85[6]
List of I/Os	Latch-up I-test	-100[2]		$-0.5xV_{DDMAX}$[4]		125
List of I/Os	Latch-up I-test	-100[2]		$-0.3xV_{DDMAX}$[5]		125
Rest of I/Os	Latch-up I-test	+/- 100[2]	$1.5xV_{DDMAX}$[4]	$-0.2xV_{DDMAX}$[5]		125
List of supplies	Latch-up Overvoltage	$1.2xV_{DDMAX}$[5]			I_{NOM} + 100	125
Rest Supplies	Latch-up Overvoltage	$1.5xV_{DDMAX}$[4]			I_{NOM} + 200	125

NOTE 1 Dedicated IO pins were not tested due to product conditioning requirement

NOTE 2 Pins stressed at Class II temperature and passed with specified I/O pin positive injection current (between 50 mA and 100 mA) and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

NOTE 3 Pins stressed at Class II temperature and passed with specified I/O pin positive injection current (less than 50 mA)and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

NOTE 4 Supplies stressed at Class II temperature and passed specified voltage injection.

NOTE 5 MSV value empirically determined to prevent an EOS-like condition.

NOTE 6 Pins stressed pass at lower Class II temperature.

Annex C (informative) Examples for recording and reporting data (cont'd)

C.2 Examples of reporting data

Example #1 for reporting data:

a) Test was performed at 125 °C case temperature (Class II).

b) I/O group #1 (V_{max}=4 V) passes +100/-200 mA I-test with clamp voltage at MSV of 5 V.

c) I/O group #2 (V_{max}=4 V) passes +200/-100 mA I-test with clamp voltage at 6 V (1.5 x V_{max}).

d) Supply groups pass 1.5 x Vccmax except the 3 V (Vccmax=3.15 V) and the 0.9 V (Vccmax=0.93 V) groups that pass MSV values of 4 and 1.2 V respectively.

e) Dedicated I/O pins were not tested due to product conditioning requirement.

f) Immunity Level A achieved.

Example #2 for reporting data with a collapsing tester supply:

a) Test was performed at 125 °C case temperature (Class II).

b) I/O group passes +100/-100 mA I-test with I_{limit} of 200mA for VDD_IO, which collapsed during positive injection.

c) Retest with higher I_{limit} I/O group passes +75mA/-100 mA I-test with I_{limit} of 800mA for VDD_IO.

d) Supply groups pass 1.5 x Vccmax.

e) Dedicated I/O pins were not tested due to product conditioning requirement.

f) Immunity Level B achieved.

Example #3 for reporting data with collapsing tester supply and reaching damage level when trying to increase I_{limit} to avoid supply collapse:

a) Test was performed at 125 °C case temperature (Class II).

b) I/O group passes +100/-100 mA I-test with I_{limit} of 1200mA for VDD_IO, which collapsed during positive injection. Further increasing I_{limit} caused damage.

c) Retest with lower I_{limit} I/ O group passes +80mA/-100 mA I-test with I_{limit} of 700mA for VDD_IO.

d) Supply groups pass 1.5 x Vccmax.

e) Dedicated I/O pins were not tested due to product conditioning requirement.

f) Immunity Level B achieved.

Annex D (informative) Differences between JESD78E and JESD78D

This annex briefly describes most of the changes made to entries that appear in this standard, JESD78E, compared to its predecessor, JESD78D (November 2011). Some punctuation changes are not included.

Clause	Description of change
Table 1	Reduced number of groups in Column 2; Added Column 4 for Immunity Level
2	cool –down time: replaced Figure 4 with Figure 6
2	maximum stress voltage (MSV): Revised text.
2	NOTE 1: Revised text.
2	NOTE 2: Revised text.
2	Vsupply pin (or pin group): Revised text.
Figure 1	Revised figure
4.1	Moved Table 3 of JESD78D to later section.
4.2	Added 4.2.1 to explain consideration of supply current limits
Figure 2	Revised timing diagram and text.
Figure 3	Revised timing diagram and text
Table 3	Table 3 of JESD78D revised with new limits and moved to 4.2.2
Figure 4	Figure 5 of JESD78D revised. Moved to clause preceding 4.2.2.
Figure 5	Figure 6 of JESD78D revised. Moved to clause preceding 4.2.2
Figure 6	Figure 4 of JESD78D. Revised.
Table 4	New table for Vsupply overvoltage level.
Figure 7	Revised and moved to 4.2.5
4.2.5	Added Ilimit settings to reporting list
Annex C	Revised with examples of recording data
Annex D	Changed Annex D to show differences between JESD78E and JESD78D
D.1	Differences between JESD78D and JESD78C
D.2	Differences between JESD78C and JESD78B
D.3	Differences between JESD78B and JESD78A
D.4	Differences between JESD78A and JESD78

D.1 Differences between JESD78D and JESD78C (September 2010)

Clause	Description of change
1	Added note to scope.
1.2	Added new text (replaced all text from previous version).
2	Added term and definition for maximum stress voltage (MSV).
4.2.5	Added new text (replaced all text from previous version).
Table 1	Renumbered Table 1 to Table 2.
Table 2	Renumbered Table 2 to Table 3.
Table 2	Table 2 (previously Table 1) changes: 1) Column 4 (Test temperature classification) – Combine Class I and II groups together to shorten the table, 2) Column 6 (Trigger test conditions for pin or supply group under test) – Text change to reflect elimination of levels and substitution with recommended characterization conditions, 3) Column 7 (Failure criteria) – Rename the column as latch-up detection criteria, 4) Footnotes 2 - Grammar correction, 5) Footnotes 3, 4 – Text change to show conditions for using maximum stress voltage (MSV); clarification of trigger current and clamping voltage polarities
5	Changed title from “Failure criteria” to “Latch-up detection criteria”
5	Replaced 1st paragraph with new text.
Annex C	Changed Annex C to Annex D. Added new Annex C.

D.2 Differences between JESD78C and JESD78B (December 2008)

Clause	Description of change
2	changed “testing of dynamic devices” to “dynamic devices”. Definition replaced, placement changed to be alphabetical.
4.1	2nd paragraph, replaced first 2 sentences.
4.1	Figure 1, replaced reference to 1.3 to 1.2
4.1	Table 1, Under “trigger test conditions” replaced reference to 1.3 to 1.2 (4 places)
4.1	Table 1, footnote 2, replaced.
4.1	Table 1, footnote 6, replaced.
4.2.2	In item 4, replaced reference to 1.3 to 1.2.
5	All of clause replaced with new material.

D.3 Differences between JESD78B and JESD78A (February 2006)

Clause	Description of change
1	Clause 1.1 combined with clause 1 to conform to JM7 Style Manual
1.2	Replace paragraph to clarify description of Class II
1.2	Clause 1.2 renumbered to 1.1 (changed references accordingly)
1.3	Clause 1.3 renumbered to 1.2 (changed references accordingly) Annex B
Annex B	Changed to Annex C. Added new Annex B.

D.4 Differences between JESD78A and JESD78 (March 1997)

At time of publication, information for annex not available.

Standard Improvement Form JEDEC _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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☐ Other _____

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