JEDEC STANDARD

Test Method for Alpha Source Accelerated Soft Error Rate

JESD89-2A

Addendum No. 2 to JESD89
(Revision of JESD89-2, November 2004)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD FOR ALPHA SOURCE ACCELERATED SOFT ERROR RATE

(From JEDEC Board Ballot JCB-07-88, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This test method is offered as standardized procedure to determine the alpha particle Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) by measuring the error rate while the device is irradiated by a characterized, solid alpha source

The results of this accelerated test can be used to estimate the alpha particle induced SER for a given alpha radiation environment. JESD89 describes considerations for executing such an estimate from data collected with this test method. Refer to JESD89 for other background on the motivation for requirements in this test method and guidance for those elements left to the discretion of the tester.

NOTE 1 This test cannot be used to project cosmic-ray induced SER.

NOTE 2 Special considerations apply to devices that are more than memory arrays and/or bistable logic elements. These can preclude the application of this test procedure. Refer to JESD89 for further discussion on some examples.

1.1 Applicable documents

JESD89	Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices
JESD89-1	Test Method for Real-Time Soft Error Rate
JESD89-3	Test Method for Beam Accelerated Soft Error Rate

2 Apparatus

The performance of this test requires equipment that is capable of providing the particular test conditions to which the test samples will be subjected.

2.1 Vehicle design and operation

The biasing and operating schemes shall consider the limitations of the devices and shall not overstress the devices or contribute to thermal runaway.

2.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under test (e.g., improper heat dissipation).

2.3 Power supplies and signal sources

Instruments (e.g., oscilloscopes) used to set up and monitor power supplies and signal sources shall be calibrated and have long-term stability. Electrical noise shielding shall be in place to allow for accurate test results.

3 Terms and definitions

DUT: Device under test.

absolute maximum rated voltage: The maximum voltage that may be applied to a device and beyond which damage (latent or otherwise) may occur. It is frequently specified by device manufacturers for a specific device and/or technology.

alpha activity (of a source): The number of alpha particles that decay in an alpha source per unit time.

NOTE The preferred SI unit is the becquerel (Bq), which is one disintegration per second. (1 curie = 3.7 x 10^{10} becquerels).

critical charge (Qc): The minimum amount of collected charge that will cause the node to change state.

3 Terms and definitions (cont'd)

flux density (of particle radiation): The time rate of flow of radiant-energy particles emitted from or incident on a surface, divided by the area of that surface.

NOTE 1 The equation **"**flux density = $N/A \cdot t$" applies, where N, A, and t represent the quantities number of particles, area, and time.

NOTE 2 The unit symbol (e.g., $cm^{-2} \cdot s^{-1}$) does not identify particle type. The particle name may be placed before the term, e.g., "neutron flux density", or in the spelled-out unit name, e.g., "neutrons per square centimeter second".

NOTE 3 Flux density is maximized when the surface is perpendicular to the direction of the incident particle flow.

hard error: An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit (e.g., gate oxide rupture, destructive latch-up events)

NOTE The error is called "hard" because the data is lost and the circuit or device no longer functions properly, even after power reset and re-initialization.

maximum operating voltage: The maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

minimum operating voltage: The minimum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

multiple-bit upset (MBU): A multiple-cell upset (MCU) in which two or more error bits occur in the same word.

NOTE An MBU cannot be corrected by a simple (single-bit) ECC.

multiple-cell upset (MCU): A single event that induces several bits in an IC array to fail at the same time.

NOTE The error bits are usually, but not always, physically adjacent.

single-event burnout (SEB): An event in which a single energetic-particle strike induces a localized high-current state in a device that results in catastrophic failure.

single-event effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic-particle strike.

NOTE Single-event effects include single-event upset (SEU), multiple-bit SEU (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE), single-event transient (SET)**,** single-event burnout (SEB), and single-event gate rupture (SEGR).

3 Terms and definitions (cont'd)

single-event functional interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).

NOTE An SEFI is often associated with an upset in a control bit or register.

single-event gate rupture (SEGR): An event in which a single energetic-particle strike results in a breakdown and subsequent conducting path through the gate oxide of a MOSFET.

NOTE An SEGR is manifested by an increase in gate leakage current and can result in either the degradation or the complete failure of the device.

single-event hard error (SHE): An irreversible change in operation resulting from a single radiation event that is typically associated with permanent damage to one or more of a device (e.g., gate oxide rupture).

single-event latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.

NOTE 1 SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.

NOTE 2 An example of SEL in a CMOS device occurs when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

single-event transient (SET): A momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by the passage of a single energetic particle.

single-event upset (SEU): A soft error caused by the signal induced by the passage of a single energetic particle.

soft error, device: An erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell.

NOTE 1 As commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process.

NOTE 2 Soft errors can be generated from SEU, SEFI, MBU, MCU, and/or SET. The term SER, which includes a variety of soft error mechanisms, has been adopted by the commercial industry while the more specific terms SEU, SEFI, etc. are typically used by the avionics, space, and military electronics communities.

soft error, power cycle (PCSE): A soft error that is not corrected by repeated reading or writing but can be corrected by the removal of power (e.g., nondestructive latch-up).

3 Terms and definitions (cont'd)

soft error, static: A soft error that is not corrected by repeated reading but can be corrected by rewriting without the removal of power.

soft error, transient: A soft error that can be corrected by repeated reading without rewriting and without the removal of power.

4 Procedure

4.1 Test duration

The test duration shall be specified by internal qualification requirements or the applicable procurement document. The test duration may be specified as the length of time to observe a minimum number of errors.

The test duration is defined as the time from the first test data write to the last test read. For static tests with test voltage above the maximum operating voltage or below the minimum operating voltage, the test write and read shall be performed at nominal voltage; immediately after the test write, the voltage shall be changed to the test voltage, and immediately before the test read, the voltage shall be changed to the nominal voltage. Care shall be taken not to induce any errors while changing the voltage. The alpha source shall be placed before the first data write and shall remain in place until after the final read.

4.2 Test conditions

4.2.1 Test voltage

Unless otherwise specified, the test voltage shall be the nominal operating voltage specified for the device. In order to characterize alpha particle SER as a function of Qcrit, lower and higher voltages are also permitted. The test voltage shall not exceed the absolute maximum rated voltage for the device and shall be agreed upon by the device manufacturer.

4.2.2 Biasing configurations

Device outputs may be unloaded or loaded to achieve the specified output voltage level. If a device has a thermal shutdown feature, it shall not be biased in a manner that could cause the device to go into thermal shutdown.

4.2 Test conditions (cont'd)

4.2.1 Test voltage (cont'd)

4.2.2.1 Alpha source accelerated SER test

Unless otherwise stated, the alpha source accelerated SER test shall be configured to provide write/read function to the entire available memory array or sensitive bistable circuit area of the device samples with insitu pass fail recording. Unless otherwise specified, the patterns or pattern suite shall consist of an equal mix of physical 1's and 0's for memory elements; this may not apply to bistable logic elements which are architected to have preferential data states. For bistable logic circuits, data shall be collected on each circuit element. For example, data collection is required to quantify the master and slave elements of a flip-flop circuit separately. Furthermore, it is recommended that the patterns or pattern suite approximate typical use.

For characterization purposes test conditions can be modified. These include supply voltages, clock frequencies, input signals, etc. which may be operated outside their specified values. When operating outside the application range of the part, predictable and nondestructive behavior of the devices under test shall be assured.

NOTE A preferred alpha source material may depend on expectations about the alpha source species and its physical distribution in the product of interest. Refer to JESD89 for guidance on these considerations. (1) Am and Th are common source species for testing; they are employed frequently to simulate Po-based decay from Pb packaging and U- and Th-based decay from a variety of mined materials, respectively. Test results should be expected to vary as function of source species. (2) Distribution of the alpha source in the packaged product can influence the preferred energy spectrum for the test alpha source. A thin-film source is often used to simulate a layer of surface contamination. A test source with a distributed energy spectrum is often used to simulate alpha emission from bulk materials.

4.3 Test sequence

A minimal test sequence shall include:

1) Test readiness check (see 4.3.1)

2) Load DUT and place alpha source

3) Initial DUT test

4) Collect data

5) Final test (see 4.3.2)

6) Repeat steps 1 though 5 for additional parts

4.3 Test sequence (cont'd)

4.3.1 Test readiness

Prior to running the SER test, a tester readiness check shall be performed without the alpha source. This check shall be performed with the hardware in the manner it will be used for the test. The tester readiness check shall verify all patterns and voltages to be used during accelerated alpha testing on the part. If the test voltage will exceed the maximum operating voltage or will be below the minimum operating voltage, the test pattern shall be written and read at nominal voltage, and the voltage shall be changed to the test voltage in the same way as during the actual test. The check is completed successfully if no errors are detected during a tester check.

This check shall be performed before any test in which the test setup or module was changed.

4.3.2 Final test for each part

For each part tested, the final test shall repeat the initial test in order to verify consistency of results. The presence of new hard fails, beyond the expected hard fail rate, or a change in the measured fail rate beyond statistical and run-to-run variations could indicate total dose effects.

4.4 Sample description

Alpha accelerated tests may be performed at wafer level or in ceramic or plastic packages. For wafer-level testing, the probe card and probe shall be designed to allow alpha source placement over the sample without shadowing the array being tested. For ceramic packages, the device die shall be mounted with the surface of the die as close as possible to the top surface of the package (see 4.5). For plastic packages, the plastic encapsulant (mold compound) shall be etched back to expose fully the chip surface. For both ceramic and plastic packages, the wirebonds shall not shadow the array or circuit area being tested. At minimum, the thickness of any polyimide coating on the sample shall be documented.

NOTE 1 Ideally, the thickness should replicate the polyimide thickness for the packaged product of interest. Otherwise, a documented approach to translate test data to a product with a different polyimide thickness is necessary..

NOTE 2 Test sites may be preferred over actual product samples where interferences (as by bumps for flip chip packaging) are significant. Refer to "6 Report" section of this document for considerations on extrapolating data collected on test sites.

4.5 Alpha source placement

After the tester readiness check, the alpha source shall be placed over the device under test (DUT). The alpha source shall remain in place throughout the duration of the SER test. The bottom surface of the alpha source shall be parallel to the top surface of the device die within 5°. Source-to-die spacing, *S*, shall be documented. In general, it is recommended that the spacing approximate the separation distance from alpha source materials in the packaged product. (NOTE: Non-zero source-to-die spacing may maximize the observed SER. Refer to JESD89 Annex D for further discussion.) In cases where the source-to-die spacing is greater than 1 mm, complete results shall account for attenuation effects. The alpha source shall be sufficiently larger than the memory array under test to allow the full angular distribution of alpha particles at the edges of the array. The required source extension past each edge of the memory array, *L*, will depend on the source-to-die spacing, *S*, the thickness of material between the active silicon and the top of the die (including metal layers, dielectric layers and polyimide, if present), *t*, and the alpha range in the material between the active silicon and the top of the die, *R*, (which depends on the source alpha spectrum and the composition of the material between the active silicon and the top of the die) as $L=(S+t)*\tan(Z)$, where $\cos(Z)=t/R$.

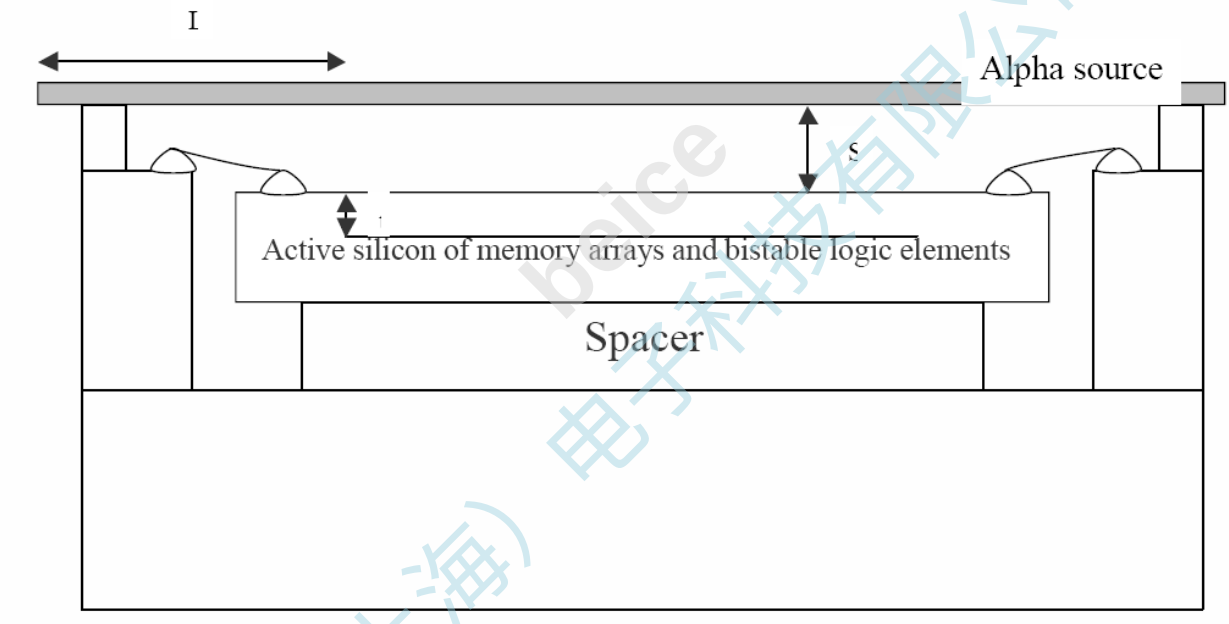

Figure 1 — Example of Alpha source placement

4.6 Handling

All testing shall follow appropriate procedures for safe handling of radioactive materials and ESD control.

4.7 Test temperature

Ambient and junction temperatures shall be recorded.

5 Failure criteria

Any result that does not match expectation is a possible soft error and shall be recorded.

Care shall be taken to minimize electrically noisy test environments and, thereby, errors related to the equipment and not the device.

Consideration shall be given to discriminating among the error types that can be encountered.

To differentiate among static soft errors, power-cycle soft errors (PCSE) and single-event hard errors (SHE), data shall be rewritten into the device and re-read. If the error is corrected by rewriting, it shall be considered a static soft error. If the error repeats after re-writing, it is not a static soft error. When an error persists after re-writing, the chip shall undergo a power-cycle where the power is removed then restored. After the power-cycle, both data states shall be written into and re-read from the faulting bits. Any faulting bits that can be written into both data states and re-read from both data states without error after the power-cycle shall be recorded as power-cycle soft errors. Faults that persist after writing into or re-reading either data state after the power-cycle shall be recorded as hard errors. PCSE and SHE shall not be counted as static or transient soft errors.

A single alpha particle can directly upset multiple memory cells. Care is required to identify multiple-cell errors. In static tests, if the total number of errors is sufficiently small so that the probability of physically proximate errors occurring from independent events remains negligible, then physically proximate errors can reasonably be assumed to be a multiple-cell upset from a single alpha particle. In dynamic runs, if 1) the tester is able to record all detected errors and 2) the time to read to whole array is small enough that the probability of physically proximate errors occurring from independent events remains negligible, then physically proximate errors can reasonably be assumed to be a multiple-cell upset from a single alpha particle. The multiple-cell error rate may be included in the final report.

Any soft error that affects multiple cells in a single read period through the memory array --and that cannot be otherwise demonstrated to be a set of independent cell errors -- shall be reported as a multiple-cells error and classified and counted according to its failure signature. The independence of cell errors can be demonstrated by distinct separation in the time of occurrence, established separation of failing physical addresses, and/or independence of the local array controls and supports for the affected cells.

NOTE An assessment of fault independence based on a distinction of tester timestamps shall consider the delay time between the event and read record. (For example, two errors caused by the same event can have different tester timestamps depending on when they are read within the read cycle of the entire chip and when the event happens within that read cycle.)

NOTE Upset of logic circuits that control reads and writes to a memory array could lead to the appearance of many cell errors. This case should be considered if there are multiple cell errors from a single event that appear to have no physical relationship in the array.

Where possible, it is desirable to identify the subset of PCSE that are SEL (as by measurement of anomalous current). Likewise where possible, it is desirable to identify the subset of static or transient soft errors that are SEFI. For memory arrays, SEFI may be distinguishable by the extent of related array addresses that are affected (as in an entire array or array subset dependent on operation of a common latch).

6 Report

The following items shall be contained in the final report for any alpha source accelerated SER test:

a) Description of each alpha source, including
   1. Isotope (e.g., Am -241, Th-232, etc.)
   2. Source alpha flux integrated over all emission angles facing the tested device; or, source alpha activity and source alpha flux calculated from source activity
   3. Source configuration (i.e., foil, diffusion bonded, etc.)
   4. Dimension and shape of source active area
   5. Description of alpha source placement, including
      i. source-to-die spacing
      ii. minimum source extension past the tested circuit area
      iii. any shadowing which obstructs the full angular distribution of alpha particles for any portion of the tested circuit area (e.g., from wirebonds or other packaging)
      iv. alignment of the source with respect to the DUT active area tested
   6. Source serial number or other identification
   7. Most recent calibration date
   8. Source alpha activity (This is measured in Becquerel or Curies and implies a integration over a spherical emission volume.)

b) Sample size (number of devices tested) and amount of array or bistable logic circuits tested on each device

c) Vehicle description, including
   1. Circuit type and subelement (e.g., SRAM, DRAM, flip-flop master, flip-flop slave)
   2. Package description (e.g., connection to chip, materials, geometries, presence and thickness of polyimide), including any modifications made for SER testing (e.g., etching plastic encapsulant to expose the chip surface)
   3. Supplier, supplier part number, and die revision (if applicable)
   4. Operational description of the circuit
   5. ECC description (type and coverage) or “tested per data sheet, ECC unknown”

6 Report (cont'd)

d) Test description, including

1. Voltage (external supply, use of internal regulated, back bias if applicable)
   NOTE Reporting an internal regulate voltage level is optional, but encouraged where the portability of the date to other devices is of interest
2. Test pattern(s), including logical data pattern and, if known, the physical data pattern
3. Test duration
4. Core cycle time or frequency or designation as "static" test with special notation of cycle times different than product data sheet
5. Refresh rate, where applicable
6. Temperature during test (at minimum, ambient temperature; if available, junction temperature as well. Report the means for determining the junction temperature.)
7. Which source, if multiple sources were used
8. Tester (commercial model and/or physical description)
9. Problems or unusual behavior of the devices during test
10. Fail information
    i. Count of each error type (transient soft errors, static soft errors, hard error)
       NOTE Because test durations are often relatively short, hard error observations are typically exceptional. Where total dose effects drive those errors, they are test artifacts only and those observations should be specially identified as such.
    ii. Identification of those soft errors that are multiple-cell errors
    iii. Electrical signature of hard errors
    iv. Failing logical address or addresses
       NOTE Interpretation of multi-cell errors is enhanced by an understanding of the physical relationship of failing addresses.
    v. Test conditions (voltage, ECC usage, data pattern, etc.) where multiple conditions are applied within the same test
    vi. Failure rate in test condition. Ideally, the failure rate should should be identified on both a per-bit (or other circuit element) basis as well as a per-event basis. At minimum, the basis for any given failure rate shall be clearly identified.
11. Periodicity of test readouts
12. The measured SER; where available, it includes the single-bit and multi-bit components and a description of how the multi-bit component was determined.

6 Report (cont'd)

If available, it is recommended to document the following information:

e) Dimensions of active area tested on the device

f) Process technology features (e.g., lithographic node, number and type of metal levels, post-metal insulators like polyimide, deep N-well, silicon-on-insulator)

g) Source energy spectrum (e.g., a list of peak energies for thin foil sources; a plot for sources with distributed spectra)
NOTE This information may be available from the supplier of the alpha source.

NOTE Refer to JESD89 for guidance on extrapolating test results to the alpha component of SER for product use. For any extrapolated product SER reported, all assumptions shall be clearly explained, including but not limited to:

i. Package description (wire bond, flip chip), materials alpha flux, and effective coverage of the material on active silicon
ii. Process layer stack (metal/dielectric) and polyimide thickness
iii. Storage device description (single-port or dual-port memory, flip-flop type, etc.)
iv. Derating factors, such as error correction circuits

Annex A (informative) Differences between JESD89-2A and JESD89-2

This table briefly describes most of the changes made to entries that appear in this standard, JESD89-2A, compared to its predecessor, JESD89-2 (November 2004). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page	Description of change

At time of publication a change page was not provided.

Standard Improvement Form

JEDEC JESD89-2A

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The referenced clause number has proven to be:

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