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ESD A/JEDEC Joint Standard

For Electrostatic Discharge Sensitivity Testing

Charged Device Model (CDM) - Device Level

Electrostatic Discharge Association
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ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Device Level

Approved February 16, 2018
EOS/ESD Association, Inc. & JEDEC Solid State Technology Association

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FOREWORD

This joint standard[1] was developed under the guidance of the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The content was developed by a joint working group composed of both ESDA and JEDEC. The new standard is intended to replace the existing charged device model ESD standards (JESD22-C101 and ANSI/ESD S5.3.1). It contains the essential elements from both standards.

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is the human body model (HBM). However, with the increasing use of automated device handling systems another potentially destructive discharge mechanism, the charged device model (CDM) becomes increasingly important. In the CDM a device itself becomes charged (e.g., by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage. It has also been shown that the CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package may be less susceptible to CDM damage at a given voltage, compared to that same IC in a package of the same type with a larger area. In fact, a new Section 7.5 and Normative Annex C address small package CDM and outlines the procedure to characterize small packages (by technology / common ESD design to those in larger packages, capacitance measurement) such that CDM testing for those small packages may not be needed.

This joint standard is a first collaborative result of combining the different CDM platform and measurement devices of both ESDA and JEDEC standards into a single platform standard document. It aims to optimize use of test systems currently in the field, while improving the waveform measurement capability in determining calibrated waveform parameters to maintain the JEDEC legacy data for use in today's systems. The key combining principle employed in this joint document is the use of current instead of voltage to define test conditions. While CDM voltages will still be reported, the underlying tester verification method uses discharge currents from the JEDEC calibration modules. This is the critical feature that allows the combination of the two former methods into one while maintaining connection to the vast majority of legacy CDM threshold data. More description of the current-based test condition approach is given in Annex C of the document. During development of this joint standard it was discovered (from waveform measurements using high bandwidth oscilloscopes) that additional ferrites (or other high frequency response modifications to the CDM test head) to meet JEDEC waveform compliance with a 1 GHz oscilloscope were being implemented in existing systems. This resulted in distortion of the actual discharge waveform. This standard now prohibits use of these components. Removal of ferrites in existing test heads or replacement of existing test heads with ferrite free versions, are both

[1] **ESD Association Standard (S):** A precise statement of a set of requirements to be satisfied by a material, product, system or process that also specifies the procedures for determining whether each of the requirements is satisfied.

straightforward modifications to ensure ANSI/ESDA/JEDEC JS-002 compliance. Additionally, initial CDM tester qualification using a high bandwidth oscilloscope is now required to ensure compliance.

This is a living document and further improvements in hardware, metrology and test procedure based on this platform are anticipated to be described in future revisions.

This standard is maintained and revised as a joint standard through a memorandum of understanding between JEDEC and ESDA. This standard is a living document and revisions and updates will be made on a routine basis driven by the needs of the electronic industry.

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ESDA/JEDEC JOINT STANDARD FOR ELECTROSTATIC DISCHARGE SENSITIVITY TESTING – CHARGED DEVICE MODEL (CDM) – DEVICE LEVEL

1.0 SCOPE AND PURPOSE

1.1 Scope

This document establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this standard. To perform the tests, the devices must be assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This test method combines the main features of JEDEC JESD22-C101 and ANSI/ESD S5.3.1. New verification procedures and test condition definitions have been introduced to facilitate this combination.

1.2 Purpose

The purpose (objective) of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms[2]

JESD99, JEDEC Standard - Terms, Definitions, and Letter Symbols for Microelectronic Devices[3]

JESD88, Dictionary of Terms for Solid-State Technology[2]

JESD625, Requirements for Handling Electrostatic Discharge-Sensitive (ESDS) Devices[2]

ANSI/ESD S20.20, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)[1]

IEC61340-5-1 – Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General Requirements[4]

3.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms available for complimentary download at www.esda.org.

charged device model electrostatic discharge (CDM ESD). An electrostatic discharge (ESD) using CDM to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal.

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[2] EOS/ESD Association, Inc., 7900 Turin Road, Bldg. 3, Rome, NY 13440-2069; 315-339-6937; www.esda.org

[2] JEDEC Global Standards for the Microelectronics Industry; www.jedec.org

[4] IEC – International Electrotechnical Commission, www.iec.ch

charged device model (CDM) electrostatic discharge (ESD) tester. Equipment (referred to as "tester" in this standard) that simulates the device level CDM ESD event using the non-socketed test method.

C_{Small}: Device to CDM field plate capacitance for an integrated circuit or discrete semiconductor at or below which it has been determined that CDM testing is not required if specified conditions are met.

dielectric layer. A thin insulator placed atop the Field Plate used to separate the device from the field plate.

field plate. A conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling (see Figure 1).

ground plane. A conductive plate used to complete the circuitry for grounding / discharging the DUT (see Figure 1).

software voltage. A user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system in order to achieve the waveform parameters as defined in Tables 1 or 2.

test condition (TC). For purposes of this document, a test condition refers to the tester plate voltage that meets the waveform parameter conditions in a particular column of Tables 1 and 2.

4.0 PERSONNEL SAFETY

DURING INITIAL EQUIPMENT SETUP, A SAFETY ENGINEER OR APPLICABLE SAFETY REPRESENTATIVE SHALL INSPECT THE EQUIPMENT IN ITS OPERATING LOCATION TO ENSURE THAT THE EQUIPMENT IS NOT OPERATED IN A COMBUSTIBLE (HAZARDOUS) ENVIRONMENT.

4.1 TRAINING

ALL PERSONNEL SHALL RECEIVE SYSTEM OPERATIONAL TRAINING AND ELECTRICAL SAFETY TRAINING PRIOR TO USING THE EQUIPMENT.

4.2 PERSONNEL SAFETY

THE PROCEDURES AND EQUIPMENT DESCRIBED IN THIS DOCUMENT MAY EXPOSE PERSONNEL TO HAZARDOUS ELECTRICAL CONDITIONS. USERS OF THIS DOCUMENT ARE RESPONSIBLE FOR SELECTING EQUIPMENT THAT COMPLIES WITH APPLICABLE LAWS, REGULATORY CODES AND BOTH EXTERNAL AND INTERNAL POLICY. USERS ARE CAUTIONED THAT THIS DOCUMENT CANNOT REPLACE OR SUPERSEDE ANY REQUIREMENTS FOR PERSONNEL SAFETY.

GROUND FAULT CIRCUIT INTERRUPTERS (GFCI) AND OTHER SAFETY PROTECTION SHOULD BE CONSIDERED WHEREVER PERSONNEL MIGHT COME INTO CONTACT WITH ELECTRICAL SOURCES.

ELECTRICAL HAZARD REDUCTION PRACTICES SHOULD BE EXERCISED AND PROPER GROUNDING INSTRUCTIONS FOR EQUIPMENT SHALL BE FOLLOWED.

NOTE: IN ADDITION, CDM TESTERS HAVE MOVING PARTS WHEN IN OPERATION AND CARE SHOULD BE TAKEN TO AVOID PERSONNEL CONTACT WITH MOVING PARTS WHEN IN OPERATION.

5.0 REQUIRED EQUIPMENT

5.1 CDM ESD Tester

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1-ohm current path with a minimum bandwidth (BW) of 9 GHz. The 1-ohm pogo pin to ground connection of the resistive current sensor may be a parallel

combination of a 1-ohm resistor between the pogo pin and the ground plane and the 50-ohm impedance of the oscilloscope and its coaxial cable. K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this standard shall meet the waveform characteristics specified in Figure 2, and Tables 1 and 2, without additional passive or active devices, such as ferrites, in the probe assembly.

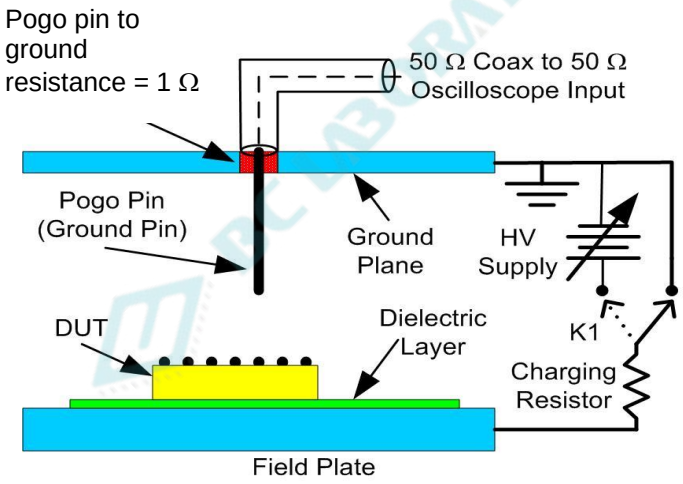


Figure 1: Simplified CDM Tester Hardware Schematic

NOTE: When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

NOTE: For existing equipment designed to meet ANSI/ESD 5.3.1 and / or JEDEC C101 standards, it is recommended to contact qualified service personnel to determine compliance to this standard upon removal of ferrite components.

5.1.1 Current Sensing Element

A current sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of 1.0 ohm ± 10%. A resistor, as specified in Section 5.1, shall be used as the current sensing element. The value of resistance (including the 50 ohm cable / oscilloscope termination) shall be measured using an ohmmeter as described in Section 5.5. The resistance value shall be used to calculate the first peak current.

The current sensing element shall have a minimum frequency response of 9 GHz (specified by maximum rolloff of 3 dB at 9 GHz).

5.1.2 Ground Plane

The probe assembly shall contain a square ground plane with the probe pin centered within it as shown in Figure 1. The dimensions of the ground plane shall be 63.5 mm x 63.5 mm ± 6.35 mm (2.5 inches x 2.5 inches ± 0.25 inches).

5.1.3 Field Plate / Field Plate Dielectric Layer

The field plate shall have a surface flatness to vary no more than ± 0.127 mm (± 0.005 inch). The field plate dielectric layer should be made with a FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0.381 mm ± 0.025 mm (0.015 inches ± 0.001 inches) in order to result in a capacitance measurement (as specified in normative Annex B) in the range specified in Table 4 in Annex A.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table 4 in Annex A.

5.1.4 Charging Resistor

The charging resistor shown in Figure 1 shall nominally be 100 megohms or greater.

Resistor values higher than 100 megohms may be used, but this may not allow very large devices (refer to Section 6.9 and Annex I) to charge fully before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 megohms, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for discharging large devices. A procedure for this large device delay characterization is given in Annex I.

5.2 Waveform Measurement Equipment

The CDM waveform measurement equipment shall consist of the following components.

5.2.1 Cable Assemblies

Cable assemblies with combined internal tester cable and external cable total loss of no more than 2 dB at frequencies up to 5 GHz and a nominal 50-ohm impedance.

5.2.2 Equipment for High Bandwidth Waveform Measurement

5.2.2.1 High Bandwidth Oscilloscope

An oscilloscope or transient digitizer with a minimum real-time (single shot) 3 dB BW of at least 6 GHz and ≥ 20 gigasample/sec sampling rate with a nominal 50-ohm input impedance.

5.2.2.2 Attenuator

A 20-dB attenuator with a precision of ± 0.5 dB, at least 12 GHz BW, and an impedance of 50 ohms ± 5.0 ohms.

5.2.3 Equipment for 1.0 GHz Waveform Measurement

5.2.3.1 1 GHz Oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 dB BW of 1 GHz with a nominal 50-ohm input impedance. The sampling rate shall be ≥ 5 gigasample/sec.

NOTE: The user has an option of using a higher BW oscilloscope and using a hardware or software filter to produce a bandwidth and sampling rate equivalent to that specified in Section 5.2.3.1.

5.2.3.2 Attenuator

A 20-dB attenuator with a precision of ± 0.5 dB, at least 4 GHz BW, and an impedance of 50 ohms ± 5 ohms.

5.3 Verification Modules (Metal Discs)

The large verification module shall have a capacitance of 55 pF ± 5% and the small verification module shall have a capacitance of 6.8 pF ± 5%. Refer to normative Annex A for information on the verification module physical dimensions and normative Annex B for information on the capacitance measurement procedure.

5.4 Capacitance Meter

Capacitance meter with a resolution of 0.2 pF, a measurement accuracy of 3%, and a measurement frequency of 1.0 MHz as described in normative Annex B.

5.5 Ohmmeter

The ohmmeter used to measure the resistance of the resistive probe shall be capable of measuring to an accuracy of 0.01 ohm. Use of Kelvin 4-wire connections is recommended.

6.0 PERIODIC TESTER QUALIFICATION, WAVEFORM RECORDS, AND WAVEFORM VERIFICATION REQUIREMENTS

6.1 Overview of Required CDM Tester Evaluations

The CDM tester shall be qualified, re-qualified, and periodically verified as described in this section. The safety precautions described in Section 4.0 shall be followed at all times.

NOTE: Dielectric layers, ground planes (ground plates), the coaxial discharging resistor (probe), the distance between the ground plane and the field plate, the verification modules and the discharge contacts (e.g., pogo pins) are key elements of the tester construction. Any change to these elements requires a waveform verification.

NOTE: Changes in the shape of the discharge pulse, even though they may still be within specification, may indicate degradation of the discharge path.

6.2 Waveform Capture Hardware

Waveform capture requires the following instrumentation and tester set voltage procedure:

- Oscilloscope - as specified in Section 5.2.
- Attenuator and cable assembly as defined in Section 5.2.
- Verification modules (as described in Section 5.3) - with the dimensions and attributes listed in normative Annex A and method of measurement listed in Normative Annex B.

6.3 Waveform Capture Setup

6.3.1 Clean the verification modules. Avoid skin contact with the modules prior to, and during testing. A recommended procedure is described in normative Annex A.

6.3.2 Using an alcohol wipe, clean the discharge probe and the field charge plate on which the device is placed to remove any surface contamination that could result in charge loss. Ensure the pogo pin is free of particulates.

6.3.3 Attach the appropriate 20 dB attenuator as described in Section 5.2 to the oscilloscope. Attach one end of the external cable assembly, as described in Section 5.2.1, to the attenuator and the other end to the CDM tester. Verify all connections in the measurement chain are tight.

See informative Annex F for an example of oscilloscope settings and captured waveforms.

6.4 Waveform Capture Procedure

6.4.1 Place the verification module to be used on the field plate dielectric, ensuring intimate contact between the field plate dielectric and verification module.

6.4.2 Set the potential of the field plate to the needed voltage for the test condition being run.

6.4.3 Align the ground pin to approximately the center of the verification module.

6.4.4 Either the single discharge or dual discharge method as described in Annex G.1 or G.2, respectively, can be used, but the discharge method chosen should be consistent with how product will be tested. When using the dual discharge method, waveforms for positive and negative pulses require a change in the oscilloscope trigger conditions to capture only positive or negative pulses.

6.4.5 Discharge the verification module at least ten times at the polarity being verified.

6.4.6 Observe at least ten successive waveforms during the set of discharges above and record the average waveform parameters for Ip, Tr, full width at half maximum (FWHM), and I_{p2} for this group of waveforms as shown in Figure 2.

6.4.7 If the waveform characteristics do not meet the requirements as defined in either Tables 1 or 2 for the target test condition (See Sections 6.5 and 6.6 for the appropriate table and test conditions to use), re-clean the verification modules and ground pin, check that all connections are tight, make adjustments in the field plate voltage and repeat steps 6.4.1 through 6.4.7.

NOTE: If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

6.4.8 Repeat the procedure for the opposite polarity.

6.5 CDM Tester Qualification/Re-Qualification Procedure

6.5.1 CDM Tester Qualification/Re-Qualification Procedure

The intent of the qualification / requalification procedure is to determine the field plate voltage needed for each test condition setting (125 – 1000) in Table 3 to produce peak current in the ranges corresponding to Table 2, and therefore corresponding to the classification levels as specified in Table 3.

Two alternative procedures for how to qualify and routinely check the CDM test system are introduced in Annex H. These procedures are based on generally available CDM test systems and offer two methods for adjusting the field plate voltage to meet the waveform parameters of Table 2.

CDM test system manufacturers, or test system operators, may develop alternate qualification procedures from the two procedures in Annex H, as long as they result in waveforms which meet the requirements of Table 2 for the various test conditions.

It is recommended that settings determined from this qualification procedure be recorded for a particular test system, oscilloscope BW and polarity. This allows for detection of drift over time on the system, which may indicate a larger issue with the system. See Section H.3 for examples.

6.5.1.1 Perform the setup and waveform capture steps as described in Sections 6.3 and 6.4 under Test Conditions 125-1000 in Table 2 for both positive and negative polarities using both small and large verification modules and measuring with the high bandwidth oscilloscope as specified in Section 5.2.2.1. Refer to Annex H for example flowcharts of the procedures.

NOTE: If local site test voltage ranges will always be narrower than the range above (for example Test Conditions 125-500), it is permissible to perform the qualification within that narrower range.

6.5.2 Conditions Requiring CDM Tester Qualification / Re-Qualification

6.5.2.1 CDM tester qualification and re-qualification as described in this section is required in the following situations:

- Acceptance testing when the CDM tester is delivered; usually performed by the manufacturer during installation.
- Periodic re-qualification in accordance with manufacturer's recommendations. The maximum time between re-qualification tests is one year.
- After service or repair that could affect the waveform.

6.5.3 1 GHz Oscilloscope Correlation with High Bandwidth Oscilloscope

6.5.3.1 During first acceptance testing, the tester manufacturer shall use a high bandwidth oscilloscope as specified in Section 5.2.2.1 for initial waveform capture. If the test site only has a 1 GHz oscilloscope as specified in Section 5.2.3.1, the tester manufacturer and end user shall confirm using appropriate bandwidth filtering techniques and comparison with the oscilloscope from the tester manufacturer that the user's oscilloscope measures tester waveforms as defined in Table 1 for quarterly and routine waveform acceptance.

NOTE: The Bessel-Thomson software filter option on many oscilloscopes is a recommended high bandwidth waveform filter as it aligns well with actual 1 GHz oscilloscope data.

6.5.3.2 Oscilloscope correlation verification shall be repeated if the test site changes 1-GHz oscilloscopes.

6.6 CDM Tester Quarterly and Routine Waveform Verification Procedure

6.6.1 Quarterly Waveform Verification Procedure

6.6.1.1 Perform the setup and waveform capture steps as described in Sections 6.3 and 6.4 under Test Conditions 125-1000 in Table 1 using the 1-GHz oscilloscope as specified in Section 5.2.3.1 or Table 2 using the high bandwidth oscilloscope as specified in Section 5.2.2.1. Both verification modules shall be checked at positive and negative polarities. Recommendation is to use the high bandwidth oscilloscope if the option exists. Refer to Annex H for example flowcharts of the procedures.

NOTE: If local site test voltage ranges will always be narrower than the range above (for example Test Conditions 125-500), it is permissible to perform the qualification within that narrower range.

6.6.1.2 Tester waveform verification shall be performed at least once per quarter.

6.6.2 Routine Waveform Verification Procedure

6.6.2.1 Perform the setup and waveform capture steps as described in Sections 6.3 and 6.4 under Test Condition 500 in Table 1 (1-GHz oscilloscope) or Table 2 (high bandwidth oscilloscope) for both positive and negative polarities using the verification module that most closely corresponds to the size package that will be tested. Refer to Annex H for example flowcharts of the procedures.

6.6.2.2 Routine Verification Frequency

Initially, upon tester qualification or re-qualification, routine waveform verification should be completed at least once per shift. If CDM stress testing is performed on consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

Longer periods between routine waveform checks may be used if no changes in waveforms are observed for several consecutive checks. The test frequency and method chosen shall be documented. If at any time the waveforms no longer meet the specified limits, all ESD stress test data collected subsequent to the previous satisfactory waveform check shall be marked invalid and shall not be used for classification.

6.7 Waveform Characteristics

The waveforms shall appear as shown in Figure 2 for both the positive polarity and its inverse for the negative polarity. The average waveform parameters (including Ip) as gathered by the method of Section 6.4 shall meet the specifications in Table 1 for a 1-GHz oscilloscope and Table 2 for a high bandwidth oscilloscope. If a high bandwidth oscilloscope is used for qualification, quarterly and routine waveform verifications, the 1 GHz requirements need not be considered.

Table 1. CDM Waveform Characteristics for a 1 GHz Bandwidth Oscilloscope

1 GHz BW Oscilloscope		Test Condition									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	Ip	1.0-1.6	1.9-3.2	2.1-3.1	4.2-6.3	4.4-5.9	9.1-12.3	6.6-8.9	13.7-18.5	8.8-11.9	18.3-24.7
Rise time (ps)	Tr	<350	<450	<350	<450	<350	<450	<350	<450	<350	<450
Full width at half maximum (ps)	FWHM	325-725	500-1000	325-725	500-1000	325-725	500-1000	325-725	500-1000	325-725	500-1000
Undershoot (A, max. 2nd peak)	Ip_2	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip

Table 2. CDM Waveform Characteristics for a High Bandwidth (> 6 GHz) Oscilloscope

>= 6 GHz BW Oscilloscope		Test Condition									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	Ip	1.4-2.3	2.3-3.8	2.9-4.3	4.8-7.3	6.1-8.3	10.3-13.9	9.2-12.4	15.5-20.9	12.2-16.5	20.6-27.9
Rise time (ps)	Tr	<250	<350	<250	<350	<250	<350	<250	<350	<250	<350
Full width at half maximum (ps)	FWHM	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900
Undershoot (A, max. 2nd peak)	Ip_2	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip

NOTE: The test condition 125-1000 voltages producing the specified peak current ranges are adjusted from JEDEC classification test voltages of 125, 250, 500, 750 and 1000 volts respectively. Tester adjusted field plate voltages to achieve these current ranges for the ferrite free tester platform in this standard may vary somewhat between testers. Informative Annex D describes this relationship between JEDEC and ferrite free tester set voltages. Informative Annex H describes two voltage adjustment methods.

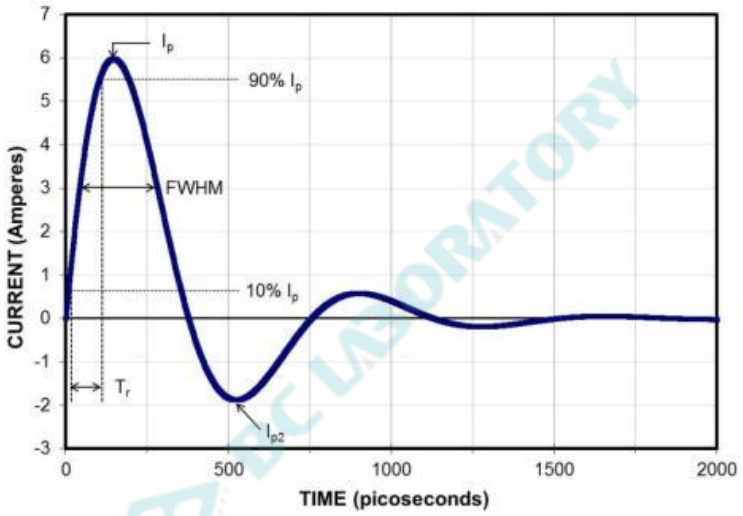


Figure 2: CDM Characteristic Waveform and Parameters

6.8 Documentation

Retain the waveform records for tester qualification according to internal company policy. For tester requalification, quarterly waveform verification and routine waveform verification, keep the records until the next set of waveforms are collected, or according to internal company policy.

6.9 Procedure for Evaluating Full CDM Tester Charging of a Device

6.9.1 As defined in Section 5.1.4, the charging resistor should nominally be 100 megohms or greater. If the resistor is too large, an added charging delay may be necessary to fully charge the device. To determine if an added delay is needed follow the procedure in Section 6.9.2.

6.9.2 Using the large verification module follow the procedure below:

1. Set the field plate voltage at + 250 volts (any voltage can be used as the objective is to monitor Ip).
2. With the pre / post charge delay both set to 0 ms, collect 10 waveforms and record the Ip from each. Calculate the average Ip of the waveforms.
3. With the pre-charge delay set to 500 ms (and post charge delay remaining at 0 ms), collect ten waveforms, record the Ip from each. Calculate their average Ip of the waveforms.
4. Compare the average Ip value from the 0 ms charge delay and the 500 ms charge delay. If the average Ip is the same for both measurements, then a device of the same or lower capacitance as the large verification module are receiving a full charge. If the average Ip with 0 ms charge delay and 500 ms charge delay do not match, refer to Informative Annex I for a procedure to determine the appropriate default charge delay to add to the system.
5. Even if the two above average Ip values match, very large packaged devices (larger capacitance than the large verification module) may still require a delay in order to receive a full charge. Since device package technologies vary widely, there are no exact dimensions for how a particular package Ip may compare to the large verification module Ip for the evaluation described above.
6. To determine if a very large packaged device may still require a charge delay, steps 1 through 4 above can be repeated using the ground pin of a device. If the average Ip with 0 ms charge delay and 500 ms charge delay do not match, refer to Informative Annex I for a procedure to determine the appropriate charge delay.

   NOTE: In addition, CDM testers have moving parts when in operation and care should be taken to avoid personnel contact with moving parts when in operation.

7.0 CDM ESD TESTING REQUIREMENTS AND PROCEDURES

7.1 Tester and Device Preparation

7.1.1 Devices used for CDM stressing shall not have been used for any prior stress tests.

7.1.2 ESD damage prevention procedures shall be used before, during, and after CDM and post parametric testing.

NOTE: See the latest revision of ANSI/ESD S20.20, JESD625, IEC61340-5-1 or company-specific handling procedures for guidance.

7.1.3 Devices shall be clean before testing. If needed, cleaning should be completed in compliance with company-approved procedures.

NOTE: Isopropanol (isopropyl alcohol) is typically used for cleaning.

7.1.4 The CDM tester probe and field plate / dielectric shall be clean and dry before testing. Cleaning may be performed periodically or based on waveform acceptance using isopropanol (isopropyl alcohol) with a minimum isopropanol percentage of 70%.

7.2 Test Requirements

7.2.1 Test Temperature and Humidity

The test shall be carried out at room temperature. Humidity at the test head should not exceed 30% RH. It is not intended to heat or cool the device during CDM testing.

NOTE: The tester should be placed in an environment where the temperature is at room temperature.

NOTE: Waveform repeatability is strongly dependent on moisture content of the air and having a low relative humidity will result in a more stable waveform.

7.2.2 Device Test

7.2.2.1 Pre-Stress Testing

Prior to ESD stressing, complete static and dynamic testing shall be performed on all submitted devices. Parametric and functional results shall be within the limits specified in the datasheet parameters.

7.2.2.2 Failure Criteria

Following ESD stressing, complete static and dynamic testing shall be performed on all stressed devices. A device is considered to have failed if parametric and functional test results are not within the limits specified in the datasheet parameters. A failure may be discounted if proven by failure analysis that it is not CDM–ESD related.

NOTE: A change in static leakage (e.g., pin leakage, standby current) is not an adequate criterion to determine pass/fail. It can serve as an indicator for the onset of damage.

NOTE: If testing is to be done at multiple temperatures, perform the test first at the lowest temperature, followed by increasing the temperature in sequence (e.g., - 40 °C, + 25 °C, + 85 °C).

7.3 Test Procedures

7.3.1 Unless otherwise specified, obtain a minimum of three samples that have been verified to meet their data specifications.

7.3.2 CDM testing should begin at the lowest level in Table 3, but may begin at any level. However, if the initial voltage level is higher than the lowest level in Table 3 and the device fails at the initial voltage, testing shall be restarted with three fresh devices at the next lower level.

7.3.3 For each device, apply at least one positive and one negative discharge to each pin. Allow enough time (as specified in Section 6.9) between discharges for the device to reach the full test voltage level. Stresses may be partitioned by polarity, using a sample size of at least three units per polarity. Pins may also be partitioned into one or more sets of samples, provided that each pin of the device is a member of at least one set. Each set shall have a minimum of three units.

7.3.4 Field-Induced Charging Method

For the field-induced charging method, there are two possible procedures for charging and discharging the device: single and dual. Both procedures produce equivalent results. These procedures are described in Informative Annex G.

7.4 CDM Test Recording / Reporting Guidelines

7.4.1 CDM Test Recording

The CDM testing procedure for a particular product shall be recorded and stored per each company's data retention procedure. Information regarding tester waveform parameters should be available upon request; refer to Annex H.3 for more information on waveform parameter recording.

7.4.2 CDM Reporting Guidelines

Product CDM test results (including package information) shall be reported and be made available in the product reliability report.

For purposes of ensuring safe handling information for manufacturing control in an ESD protected area, it is highly recommended that publicly available product datasheets report CDM classifications.

7.5 Testing of Devices in Small Packages

Integrated circuits and discrete semiconductors (ICDS) in very small packages are very difficult to test for CDM and seldom fail CDM testing due to their small capacitance. It is not possible to specify a package dimension below which CDM testing is not needed as different technologies, design styles, and protection strategies have different susceptibilities to charged device events. In the absence of other information, all ICDS shall be tested. However, Annex C defines an optional procedure for establishing an integrated circuit capacitance C_{Small} for a specific technology and design flow. For devices with capacitance below C_{Small}, CDM testing is no longer required. ICDS with capacitance below C_{Small} and which satisfy the requirements of Annex C shall be considered to have a CDM passing level of TC 750 (Classification Level C2b in Table 3).

8.0 CDM CLASSIFICATION CRITERIA

ESD sensitive (ESDS) devices are classified according to the test procedure described in this standard. CDM test results are specific to the particular package type used. The device classification is the highest ESD stress voltage level (both positive and negative polarities) at which a sample of at least three devices has passed full static and dynamic testing per data sheet parameters following ESD testing. The CDM ESDS device classification levels are presented in Table 3.

Table 3. CDM ESDS Device Classification Levels

Classification Level (see Note 1)	Classification Test Condition (in Volts) (See Note 2)
C0a	< 125
C0b	125 to < 250
C1	250 to < 500
C2a	500 to < 750
C2b	750 to < 1000
C3	≥ 1000 (see Note 3)

NOTE 1: Use the "C" prefix to indicate a CDM classification level.

NOTE 2: The Classification Test Condition is not equivalent to the actual set voltage of the tester. Please see Section 6.5.1 and Annex H for further details.

NOTE 3: For Test Conditions above 1,000 volts, depending on geometry of the device package, corona effects may limit the actual pre-discharge voltage and discharge current.

ANNEX A (NORMATIVE) – VERIFICATION MODULE (METAL DISC) SPECIFICATIONS AND CLEANING GUIDELINES FOR VERIFICATION MODULES AND TESTERS

A.1 Tester Verification Modules and Field Plate Dielectric

The verification modules (metal discs) shall be made of brass, plated with nickel or gold / nickel, and may optionally have a gold flash coating over the nickel. They shall be manufactured to the dimensions specified in Table 4 and shall be verified once before the initial use by either the manufacturer or user.

NOTE: Caution should be exercised during the manufacture of the discs so that they are free from “burrs”. If the perimeter of the disc has “burrs”, arcing may occur which may alter the results.

The field plate dielectric is chosen (see Section 5.1.3) to result in a capacitance measurement in the range specified in Table 4.

Table 4 – Specification for CDM Tester Verification Modules (Metal Discs)

Disk	Small	Large
Diameter mm (inches)	8.89 ± 0.127 (0.350 ± 0.005)	25.4 ± 0.127 (1.000 ± 0.005)
Thickness mm (inches)	1.27 ± 0.05 (0.05 ± 0.002)	1.27 ± 0.05 (0.050 ± 0.002)
Surface flatness variation mm (inches)	≤ 0.127 (0.005)	≤ 0.127 (0.005)
Capacitance at 1 MHz (pF)	6.8 ± 5%	55 ± 5%

A.2 To avoid charge loss in verification modules during charged device model (CDM) evaluation, the verification modules should be cleaned using isopropanol (isopropyl alcohol, IPA) swabs for about 20 seconds as approved by the local safety organization and dried in a moderate air stream to prevent charge leakage during test operation. Verification modules should be handled so as to maintain cleanliness.

The capacitance of the small and large verification modules (metal discs) shall be measured according to the procedure in Annex B and shall conform to the values specified in Table 4.

The tester should be cleaned periodically with isopropanol to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe and field plate dielectric on which the device is placed.

NOTE: Cleaning with isopropyl alcohol swabs may leave the surface moist for some period of time after the cleaning. The moisture may provide an unintended leakage path if present during the test. It is important to dry all surfaces after cleaning either by allowing sufficient time for the surfaces to dry or using forced air flow to evaporate the moisture.

ANNEX B (NORMATIVE) – CAPACITANCE MEASUREMENT OF VERIFICATION MODULES (METAL DISCS)

B.1 Capacitance of Verification Module Sitting on Tester Field Plate Dielectric

B.1.1 The capacitance of the verification modules shall be measured in-situ (inside the CDM simulator) but can also be measured outside of the CDM simulator as guidance.

B.1.2 The small verification module is placed on the dielectric layer which is in direct contact with the surface of the grounded metallic field plate. Ensure there is no air space between the module and the dielectric layer, and also no air space between the dielectric layer and the metallic field plate.

NOTE: It is recommended that vacuum be used to ensure the verification module is held in place against the field plate dielectric.

B.1.3 Ensure the capacitance meter is "zeroed out" prior to measurement.

Connect the two leads from the capacitance meter (CP) as follows. One metallic lead/cable from the CP is connected to an exposed point on the field plate. The second metallic lead/cable from the CP is connected to the top of the verification module (in the center).

B.1.4 Measure the capacitance of the module to the grounded field plate. The capacitance value of the verification module shall be within the value specified in Annex A, Table 4.

B.1.5 Repeat Sections B.1.1 to B.1.4 using the large verification module on the dielectric.

NOTE: Placement of the CP meter leads can cause changes in the measured capacitance. One recommended technique for each verification module is to make a first measurement as outlined in Section B.1.4 and then make a second measurement with the verification module lead/cable just above, but not touching, the verification module. The second reading is subtracted from the first to result in the true measured value.

NOTE: A meter with "guarded leads" is recommended for use.

ANNEX C (NORMATIVE) – TESTING OF SMALL PACKAGE INTEGRATED CIRCUITS AND DISCRETE SEMICONDUCTORS (ICDS)

This annex describes a procedure for setting a capacitance limit C_{small}, below which small package integrated circuits and discrete semiconductors no longer need to be tested for CDM. ICDS in very small packages are very difficult to test, due to the challenge of handling small devices. Very small ICDS also have very low capacitance to surroundings, including during CDM testing. With a small capacitance very little charge is transferred during a CDM event, either in a factory environment or during CDM testing. Small package ICDS therefore seldom fail during CDM testing. This does not, however, mean that there is no CDM risk for small package ICDS. The charge transferred during a small package CDM event may be small but the peak currents remain high, usually over an amp since the RLC equivalent circuit of a CDM event results in a very narrow, but still high current pulse. It is very difficult to set a minimum package dimension or capacitance for CDM testing because CDM failure levels depend on a wide variety of variables, including those listed below.

- Capacitance between the ICDS and the field plate
- The technology used to fabricate the device
  - Advanced low voltage technologies have thin gate oxides with low breakdown voltage and may be more susceptible to CDM damage without a proper protection scheme
  - High voltage technologies have diffusions which can be subject to CDM damage
- ESD protection circuits used in the device
- General ESD protection strategy used
- Design style used to design the device
- Thoroughness of ESD design rule checks
- Package type which can influence inductance in the CDM current path

C.1 Procedure for Determining C_{Small}

The following procedure may be used to determine a limit, C_{small}, at and below which CDM testing is not required for a particular integrated circuit technology.

- Choose at least 5 ICDS designs from a technology, with varying package sizes
  - The requirements for circuits to be considered from the same technology are given in Section C.2
- Measure the capacitance between each ICDS substrate, usually the ground pin, and the CDM tester's field plate when the ICDS is in the position for CDM testing, using the procedure in Annex B for measuring the capacitance of the verification modules.
  - Packages shall be at least 4 times the size of the vacuum hole in the dielectric layer or the metal field plate, whichever is larger. If the package is less than 4 times the size of the vacuum hole a test fixture which holds the package against the dielectric should be used. At this time, there is no universally recognized method for testing CDM capability on packages that are less than 4 times the size of the vacuum holes. Techniques including mechanical methods for holding the package made of FR4 with the package not over vacuum holes, or packaging die in a different package, have been used.
  - A separate test fixture may be used for measuring the capacitance if it uses the same thickness and material for the field plate dielectric layer as the CDM tester
- Perform CDM testing at TC 1000 for 3 samples as per Section 7.3.3 for each of the 5 ICDS designs.
- The ICDS capacitance, at which all ICDS with that capacitance and lower all pass CDM TC 1000, is C_{Small}.

NOTE: To ensure there is no air space between the integrated circuit and the dielectric layer, and also no air space between the dielectric layer and the metallic field plate, the use of vacuum is recommended.

ICDS with substrate to CDM tester field plate capacitance equal to or less than C_{Small} do not need to be tested for CDM if the following conditions are met:

- The ICDS has passed HBM according to requirements of the technology. This indicates the expected protection circuit is present.
- The ICDS uses the same technology, as defined in C.2, as used to determine C_{Small}

- ICDS devices not tested because their capacitance is below C_{Small} and satisfy the above requirement shall be considered to have a CDM passing level of TC 750 (Classification Level C2b).

C.2 ICDS Technology Requirements

ICDS are considered to be from the same technology if the following conditions are met:

- The ICDS must use the same wafer fabrication flow
- All ICDS must use the same ESD protection circuits and ESD design rules.
- All ICDS must have their substrate to CDM tester field plate capacitance measured using the procedures in Annex B
  - A separate test fixture which simulates the CDM tester field plate and dielectric may be used
  - Calculated substrate to field plate capacitance may be used if the calculation procedure has been verified with measurements using the procedures in Annex B.

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2018)

ANNEX D (INFORMATIVE) – CDM TEST HARDWARE AND METROLOGY IMPROVEMENTS

D.1 CDM Test Hardware and Metrology Improvements

The goal of the new joint ESDA/JEDEC CDM standard is to reduce duplication of effort and confusion by developing a single joint work in progress, correct deficiencies in the existing CDM standards and maintain similar stress levels as the JEDEC CDM standard, since it is the most widely used CDM test method. This required significant hardware and metrology changes to arrive at an improved joint work in progress. This informative annex describes the motivations for these updates.

The major changes in this test method are listed below.

- Modified details of the required waveforms to better match the high frequency behavior of CDM events.
- Requires that the test head not include ferrites or other circuits to modify the high frequency behavior of the CDM pulse.
- Requires that tester qualification and requalification be performed with a 6 GHz or faster oscilloscope and recommends the use of 6 GHz or faster oscilloscopes for quarterly and regular tester verification if a fast oscilloscope is available.
- The tester qualification and verification procedures have been modified to give more flexibility in the field plate voltage settings to arrive at the required peak currents.
- The specification of test levels by voltage has been replaced by a series of test conditions which are related to the legacy JEDEC CDM voltage levels.

When the original CDM test method was developed in the late 1980s, single shot oscilloscopes with 1 GHz and higher bandwidths were expensive, not readily available and less capable than those available today. The result was that the original waveforms used to develop the JEDEC CDM standard had a wider half width than was characteristic of the actual CDM event. As measurement capability improved and the high frequency behavior of test heads was improved, tester manufacturers found the peak width at half height was narrower than allowed by the JEDEC standard. In order to meet the peak width at half height, ferrite beads were often added to the test head to bring the current waveforms into compliance. When oscilloscopes in the 4 to 8 GHz range become readily available it was found that the ferrite beads, which simply broadened the peak width when measured with a 1 GHz oscilloscope, created undesirable high frequency harmonics with undesirable consequences. A primary goal in the development of this standard was to remove the ferrite beads from the CDM test heads and to modify the waveform requirements to allow this change.

The 1 GHz oscilloscope specified in the JEDEC standard, and allowed in the ESDA standard, is only marginally fast enough to capture CDM events and significantly reduces the measured peak current of the captured waveforms, especially for the small verification module and small integrated circuits. Accurate peak current measurements require the use of a measurement chain with 6 GHz or higher bandwidth, and the new Joint Standard reflects this requirement for CDM tester qualification. A 1 GHz oscilloscope was considered adequate for routine waveform verification, and that option is still available in the new standard; although the higher bandwidth oscilloscope is recommended if it is available.

The increased flexibility between the required peak current values and the field plate voltage to produce the peak current has been implemented for two reasons; to better match current practice and to achieve similar stress levels as the legacy JEDEC standard.

Both the JEDEC and ESDA standards specified the CDM tester geometry as well as the required waveforms at specified field plate voltages. CDM tester manufacturers quickly found that it was often impossible to obtain the required peak current values with the required geometry and the specified field plate voltage. The manufacturers introduced adjustments to the field plate voltage so that the required waveforms were obtained when the specified voltage was selected in the CDM tester software. This adjustment was reasonable since it is known that it is peak current, not field plate voltage, which damages integrated circuits. The result was that when an integrated circuit

passed 500 volts the field plate voltage was often considerably different than 500 volts, but the intended current pulse was in fact applied to the device under test.

The removal of the ferrite beads, and the extra impedance which the beads produced, has resulted in higher peak currents than were present in the legacy JEDEC test method for the same field plate voltage and tester geometry. This creates a second reason to give more flexibility in the setting of the field plate voltage to obtain the required peak currents. Since CDM failure is a result of the peak current during the CDM event, it is therefore more important that different CDM testers create the same peak current for specified test conditions than that the field plate voltages are the same. For this reason, the test voltages specified in the earlier standard CDM documents have been replaced by a series of test conditions producing peak currents similar to those at the specified voltages in JEDEC JESD22-C101.

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2018)

ANNEX E (INFORMATIVE) – CDM TESTER ELECTRICAL SCHEMATIC

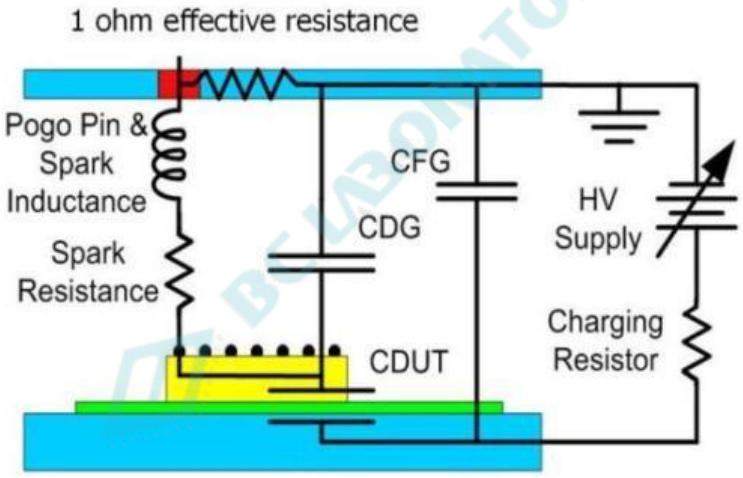


Figure 3: Simplified CDM Tester Electrical Schematic

Figure 3 represents an electrical model of a CDM tester setup. CDUT is the capacitance between the DUT and the field plate, CDG is the capacitance between the DUT and the ground plane and CFG is the capacitance between the field plate and the ground plane. The 1-ohm resistance between the pogo pin and the ground plane may be the parallel combination of the resistive probe and the coaxial cable / oscilloscope impedance as described above. The resistance of the spark which forms between the pogo pin and the DUT is assumed to be a variable resistance. The inductance of the pogo pin and spark are lumped together as a single inductor.

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2018)

ANNEX F (INFORMATIVE) – SAMPLE OSCILLOSCOPE SETUP AND WAVEFORM

The following setup examples are based on measurements of a TC 500 waveform using a 1 GHz and 8 GHz oscilloscope. Other oscilloscopes will have different settings, but this annex should provide basic guidelines that can be used on most oscilloscopes.

F.1 Settings for the 1 GHz Bandwidth Oscilloscope

Vertical: 200 millivolts / division (small verification module) or 200 millivolts / division (large verification module)

Timebase: 400 ps / division

Trigger: 300 millivolt small verification module or 400 millivolt large verification module

Impedance = 50 ohms

NOTE: These settings are for an oscilloscope for which the attenuation correction could not be made.

F.2 Settings for the High Bandwidth Oscilloscope

Vertical: 2 volts / division (small verification module) or 2 volts / division (large verification module)

Timebase: 400 ps / division

Trigger: 3-volt small verification module or 4-volt large verification module

Impedance = 50 ohms

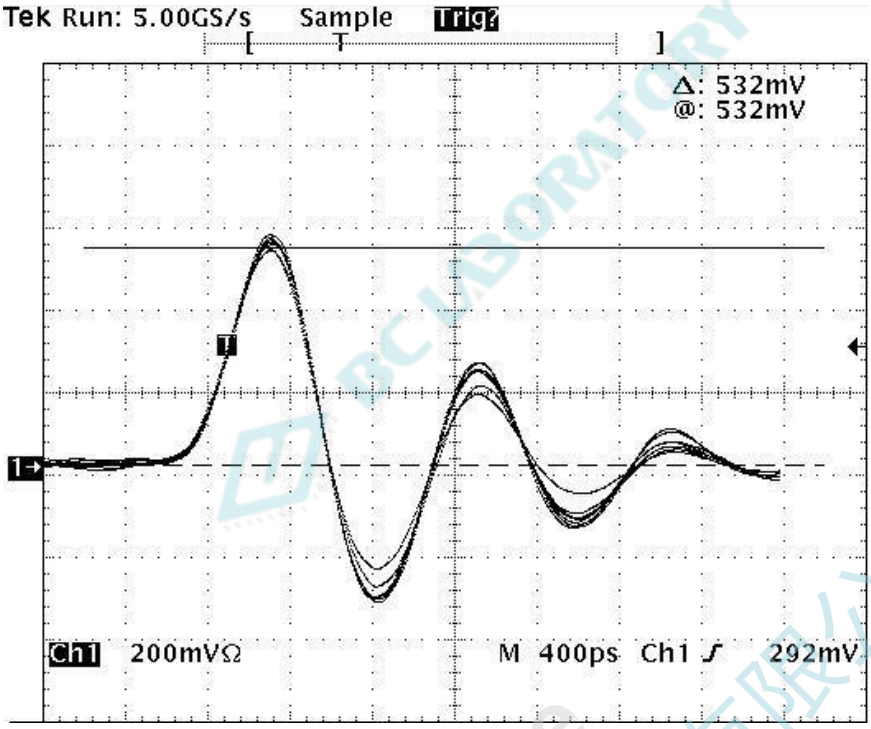
NOTE: These settings are for an oscilloscope for which the attenuation correction was made in the oscilloscope software.

F.3 Setup

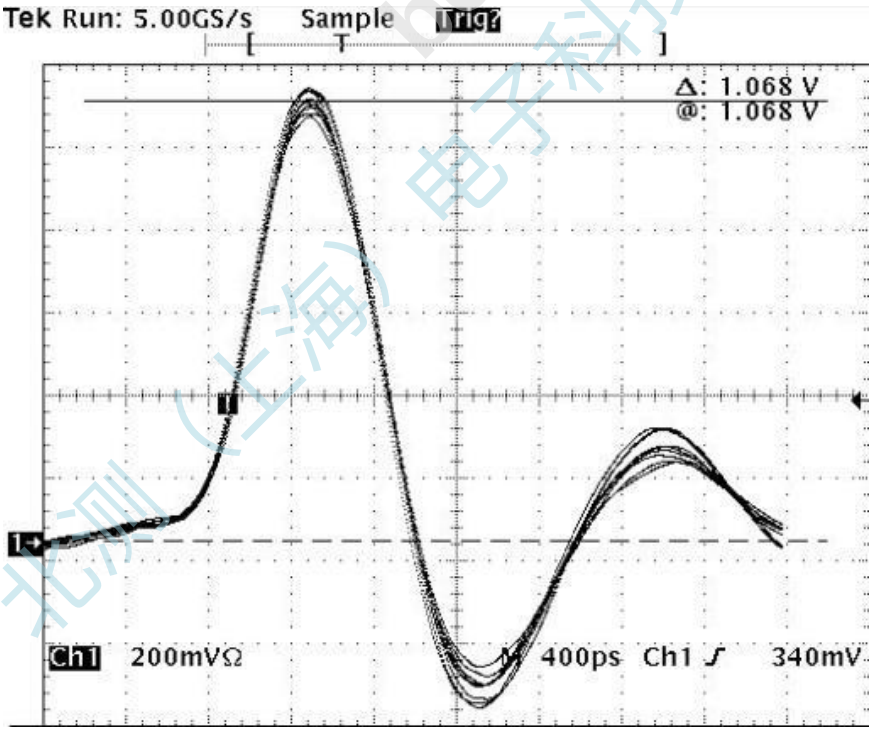
Attach the 20-dB attenuator to the oscilloscope. Attach the cable to the end of the attenuator and to the voltage output of the CDM tester.

NOTE: The 20-dB attenuator is a 10X attenuator. If the oscilloscope does not automatically compensate for this, the measurements need to be multiplied by 10 to get the correct reading (e.g., from small coin below 532 millivolts = 5.32 amperes peak current).

F.4 Sample Waveforms from a 1 GHz Oscilloscope



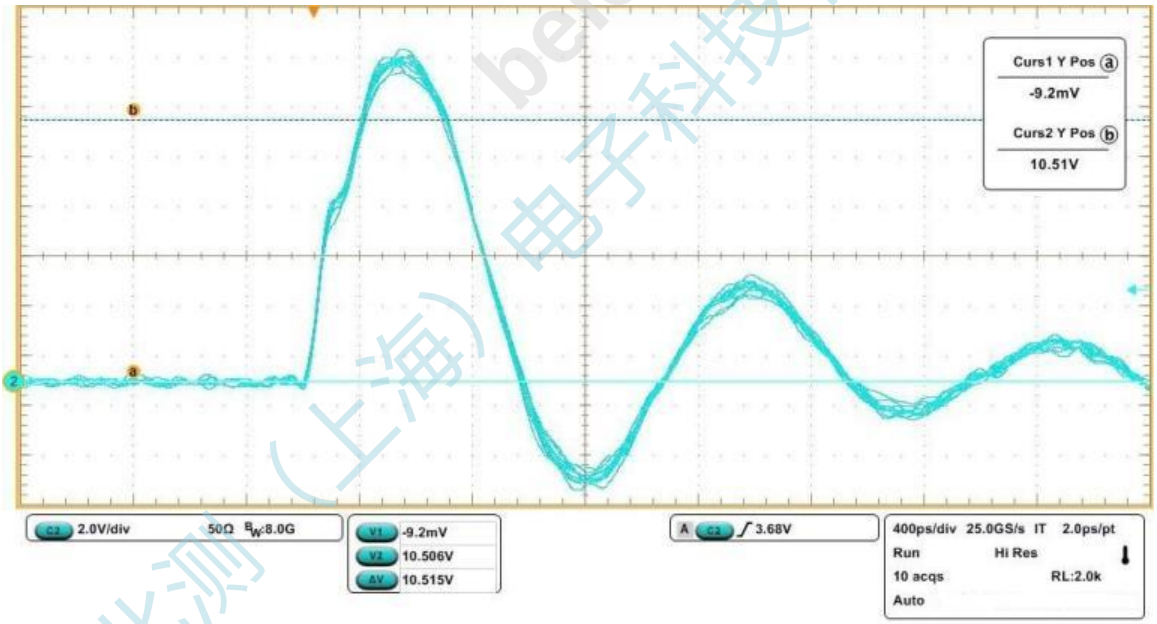
1 GHz TC 500, Small Verification Module



1 GHz TC 500, Large Verification Module

F.5 Sample Waveforms from an 8 GHz Oscilloscope

8 GHz TC 500, Small Verification Module (oscilloscope adjusts for attenuation)



8 GHz TC 500, Large Verification Module (oscilloscope adjusts for attenuation)

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2018)

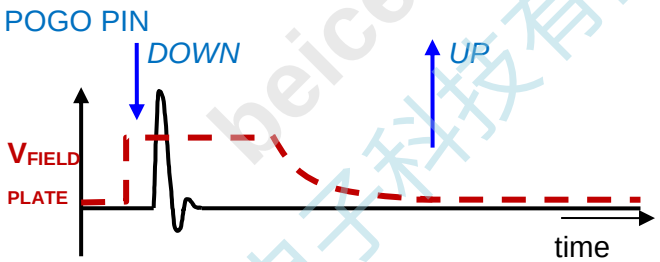
ANNEX G (INFORMATIVE) - FIELD-INDUCED CDM TESTER DISCHARGE PROCEDURES

This annex describes the two types of discharge procedures used in field-induced CDM test equipment.

G.1 Single Discharge Procedure

The single positive and single negative discharges can be applied with two individual discharges using this sequence of steps producing the sequence of charging / discharging events as illustrated in Figure 4.

a. Place the uncharged DUT on the field plate and align it.
b. The field voltage is established by raising the voltage on the field plate to the specified stress level.
c. The first discharge is made by lowering the pogo pin to the DUT (see Figure 4).
d. The pogo pin continues to descend until it makes physical contact with the device pin under test (PUT) to ensure full charge transfer and to provide a conduction path to ground.
e. Then the voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge that was transferred to the DUT during the first CDM discharge.
f. The pogo pin is returned to its starting (separated) position (see Figure 4) before the voltage of the same or opposite polarity is applied to the field platefor subsequent discharges.
g. Repeat for each pin to be tested.



Field plate ($V_{FIELD\ PLATE}$ dashed line) at High Voltage (+) before DUT is contacted by pogo pin, and at Zero before raising the pogo pin

Figure 4: Single Discharge Procedure (Field Charging, I_{CDM} Pulse, and Slow Discharge)

G.2 Dual Discharge Procedure

The single positive and single negative discharges can be applied with one pair of alternating polarity discharges using this sequence of steps producing the sequence of charging / discharging events as illustrated in Figure 5.

a. Place the uncharged DUT on the field plate and align it.
b. The field voltage for the positive stress is established by raising the voltage on the field plate to the specified stress level.
c. The first discharge is made by lowering the pogo pin to the DUT (see Figure 5).
d. The pogo pin continues to descend until it makes physical contact with the DUT. This is to ensure full charge transfer and to provide a conduction path to ground.
e. The pogo pin is returned to its starting separated position (see Figure 5), leaving the device with a net charge.

f. The voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge on the field plate. The DUT will still have a net charge.

g. The pogo pin is lowered (the second down arrow to the right in Figure 5) a second time for the second discharge, which will be of opposite polarity and the same magnitude.

h. Repeat for each pin to be tested.

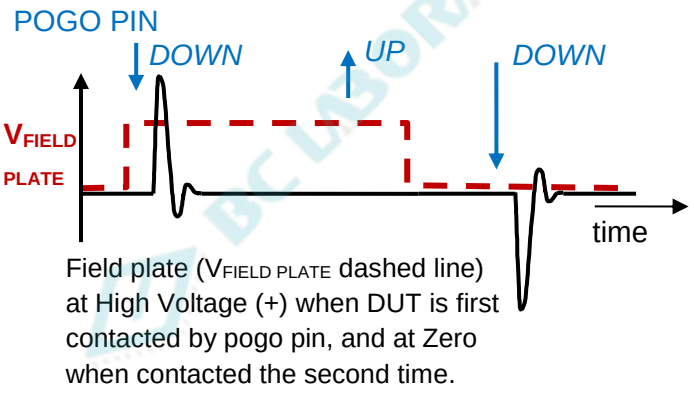


Figure 5: Dual Discharge Procedure (Field Charging, 1st I_{CDM} Pulse, No Field, 2nd I_{CDM} Pulse)

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2018)

ANNEX H (INFORMATIVE) - WAVEFORM VERIFICATION PROCEDURES USING FACTOR/OFFSET ADJUSTMENT METHOD

This procedure aligns the tester for direct software voltage input of the test condition for the full alignment range. This method may not allow for alignment of each test condition with the target mid-range of Ip as shown in Tables 1 or 2, but it is the easiest to use in a lab environment with multiple testers, as the software voltage entered matches the test condition target level and does not require linear interpolation/extrapolation for test conditions other than the five levels listed in Tables 1 or 2.

The requirements/details of this method are as follows:

- A single factor/offset is used across the entire test condition range.
- A different factor/offset can be used for each polarity.
- The same factor/offset must be used for both large and small verification modules.

Figure 6 below depicts the waveform verification flow for qualification/re-qualification and quarterly checks, while Figure 7 shows the flow for routine verifications. Annex H.3, Table 5, shows an example of the data which should be recorded.

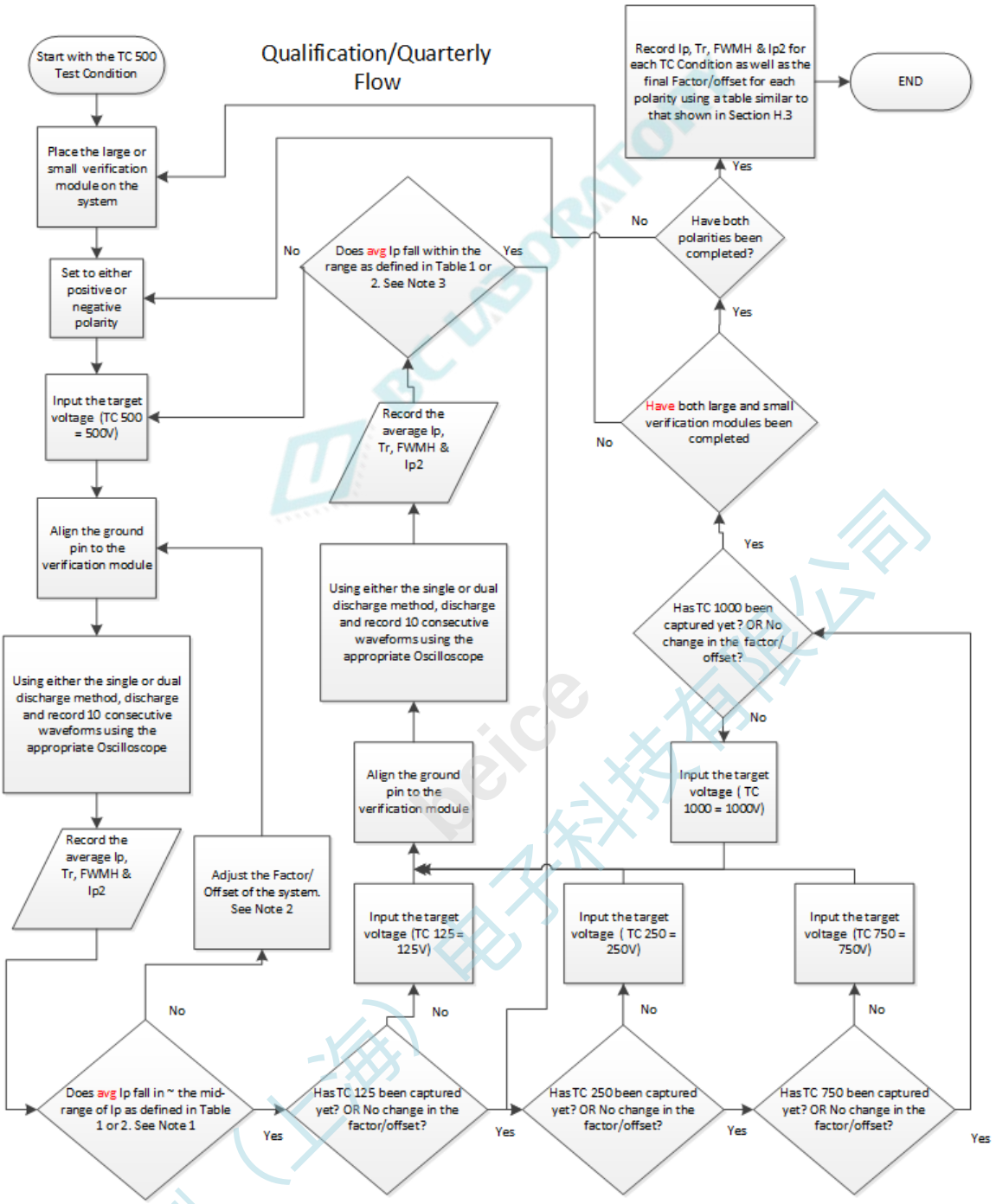


Figure 6: Example of a Waveform Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

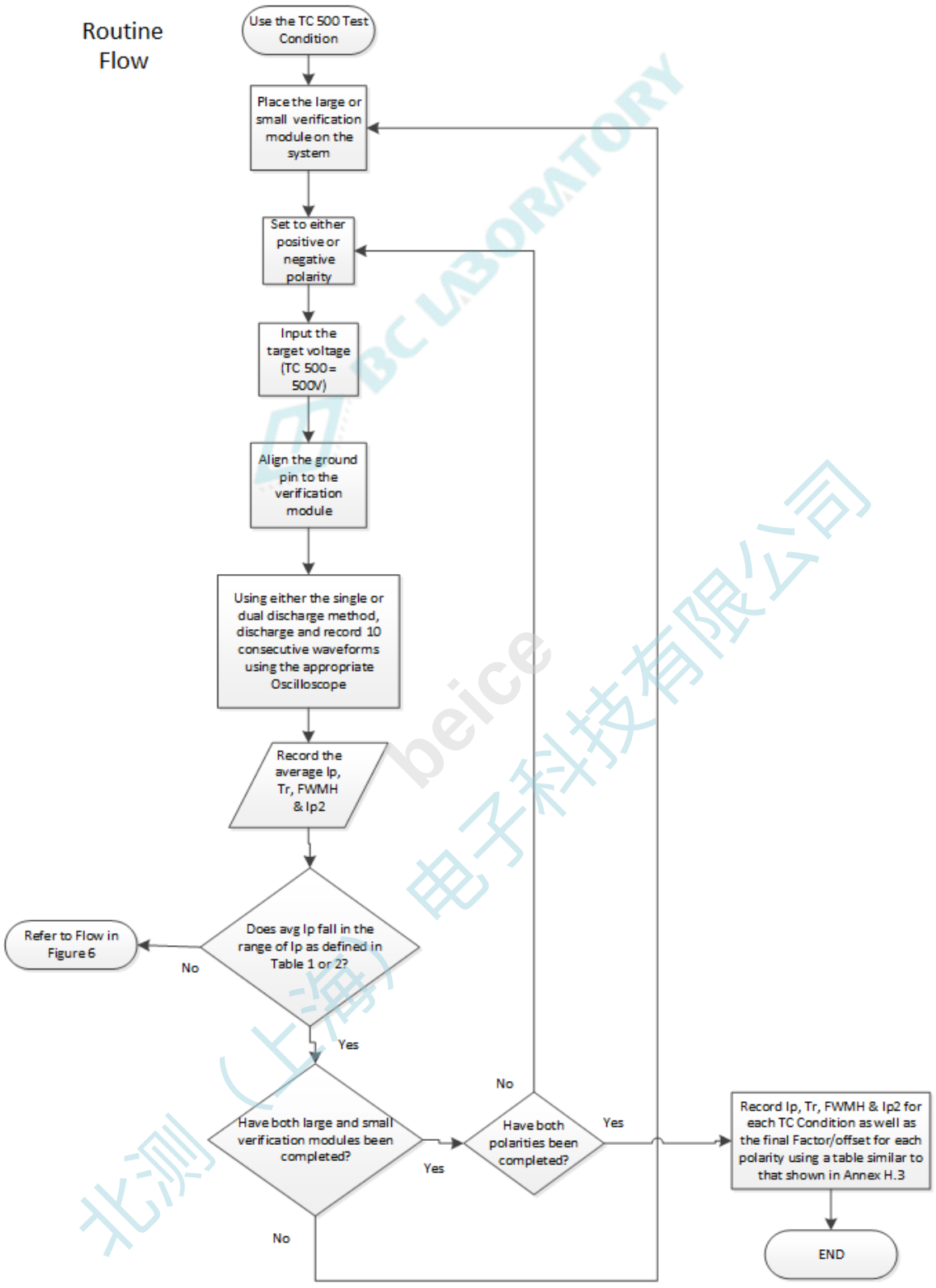


Figure 7: Example of a Waveform Verification Flow for the Routine Checks Using the Factor/Offset Adjustment Method

NOTE 1: Targeting to the mid-range of TC 500 is a starting point for adjustment of the field plate voltage. Based on the results of the other test conditions (TC 125/250/750/1000) the Ipeak may end up higher or lower than the mid-range value on TC 500. As shown in Figure 8, adjustments in the factor/offset may shift the Ipeak higher or lower.

NOTE 2: To properly calibrate systems, tester manufacturers have implemented a secondary "adjustment" parameter as an offset from the software voltage setting, either represented as a voltage "multiplier" value or a percentage "offset" value which modifies the field plate voltage. Consult the tester manufacturer for more detail.

NOTE 3: After several iterations through this loop, if the user finds they cannot meet the Ipeak range as defined in Tables 1 or 2 or the factor/offset is outside the typical documented range, re-clean the verification modules and ground pin and check that all connections are tight. If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

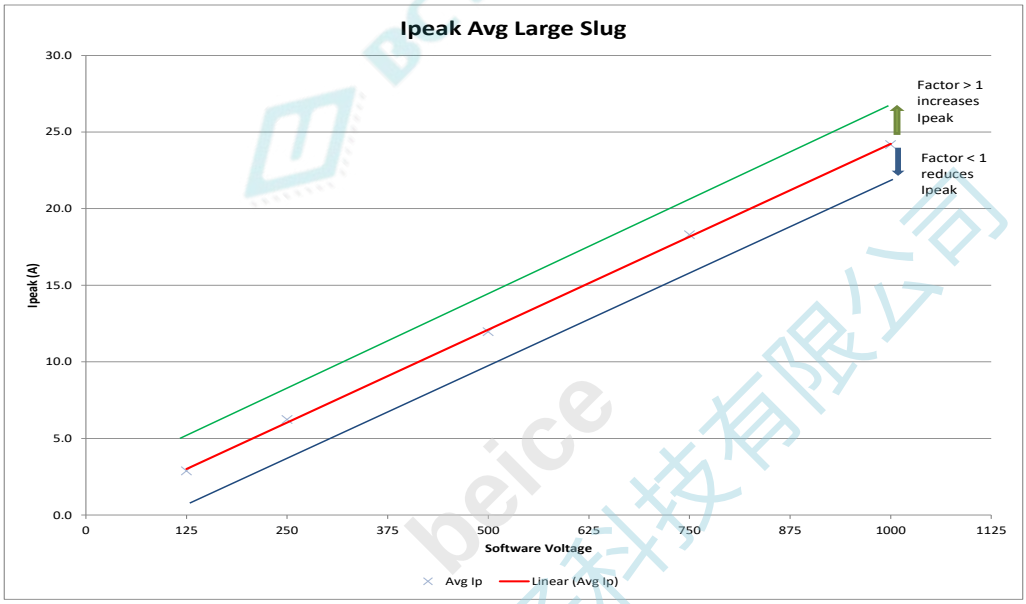


Figure 8: Example of Average Ipeak for the Large Verification Module – High Bandwidth Oscilloscope

H.2 Software Voltage Adjustment Method

This procedure does not adjust the factor/offset but leaves the factor/offset with a value that will not impact the field plate voltage and uses the software voltage entry as the primary adjustment of the field plate voltage. This method will allow for a much more accurate targeting of the midpoint of the Ip range as defined in Tables 1 or 2 but creates complexity in determining the correct software voltage entry between the five Test Conditions. Determining software voltage entries, other than the five test condition levels, (which will be determined in this procedure) will require linear interpolation / extrapolation.

The requirements/details of this method are as follows:

- A unique software voltage setting is determined for each Test Condition.
- Unique voltage settings may be used for each polarity (at each Test Condition).
- The same software voltage setting must be used for both large and small verification modules at each Test Condition.
- Testing at levels other than the five Test Conditions will require a linear interpolation / extrapolation to determine the correct software voltage entry.

Figure 9 below depicts the waveform verification flow for qualification/re-qualification and quarterly checks while Figure 10 shows the flow for routine verifications. Annex H.3, Table 6, shows an example of the data which should be recorded.

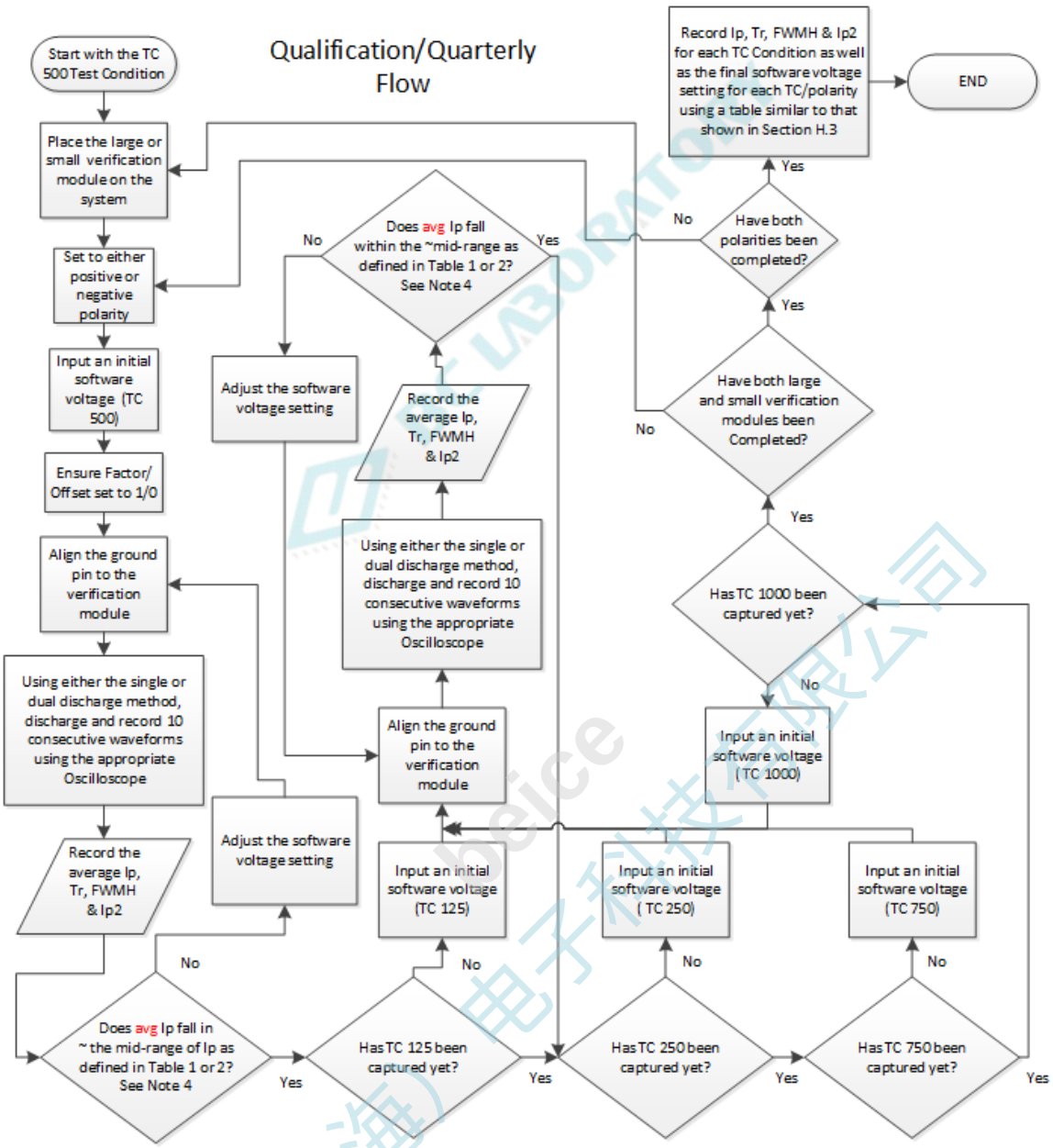


Figure 9: Example of a Waveform Verification Flow for Qualification and Quarterly Checks Using the Software Voltage Adjustment Method

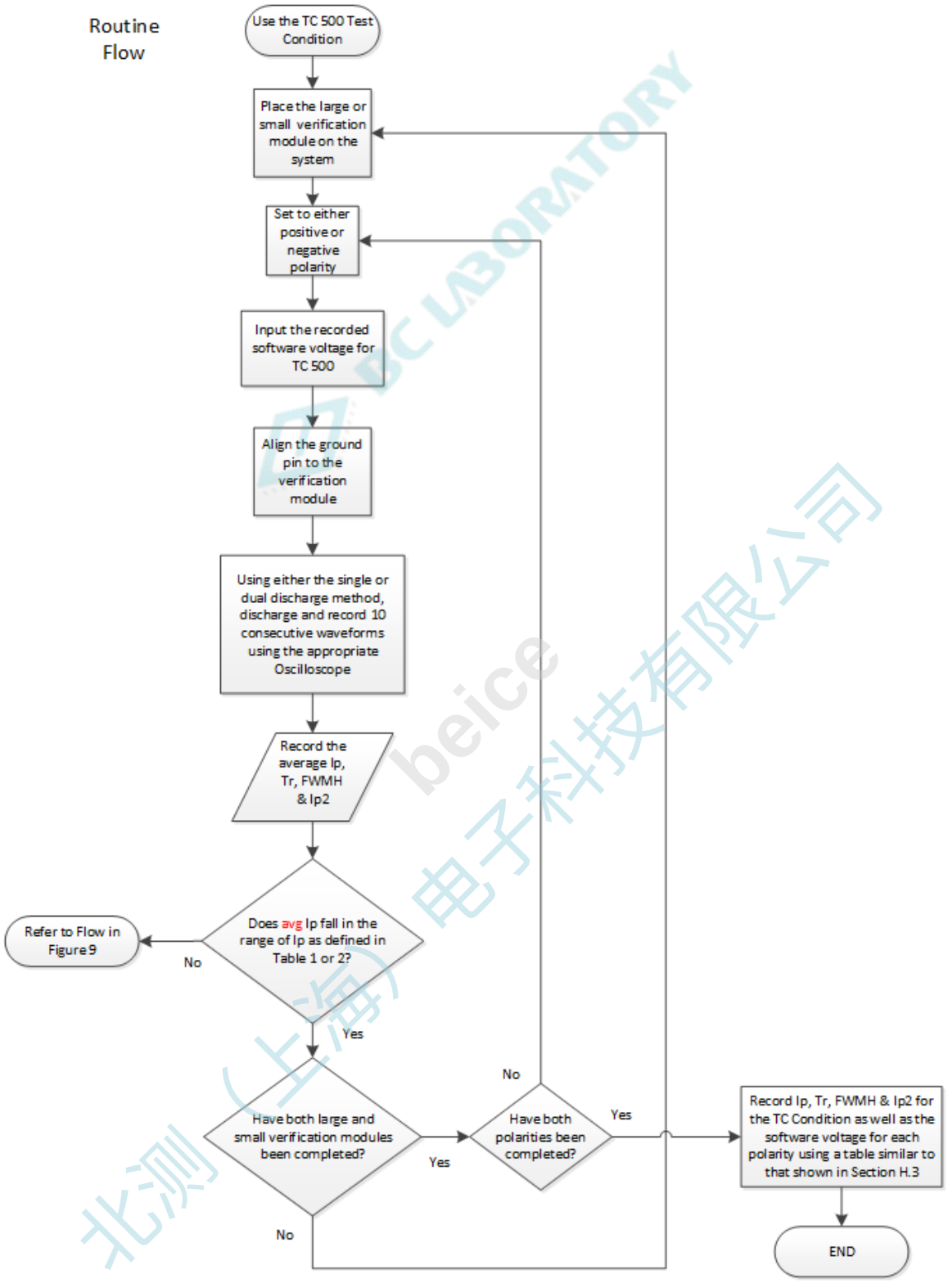


Figure 10: Example of a Waveform Verification Flow for the Routine Checks Using the Software Voltage Adjustment Method

NOTE: After several iterations through this loop, if the user finds they cannot meet the Ipeak range as defined in Tables 1 or 2 or that the software voltage setting is well outside the typical documented range, re-clean the verification modules and ground pin and check that all connections are tight. If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

H.3 Example Parameter Recording Tables

Below is an example table of CDM qualification / quarterly verification waveform parameters to be recorded for the factor/offset adjustment method.

Table 5. Example Waveform Parameter Recording Table for the Factor/Offset Adjustment Method

Tester - System #1									
Polarity = Positive		Scope Bandwidth = 8 GHz				Factor/Offset Final Setting = 0.82			
MODULE SIZE	DATE	%RH	Test Cond	Software voltage	$I_{P\ AVG}$ (A)	$T_{R\ AVG}$ (ps)	$T_{D\ AVG}$ (ps)	$I_{P2\ AVG}$ (A)	I_{P2} (% I_{P1})
Large	dd/m/yy	X%	TC 500	500	12.1	275	610	4.3	36%
Small	dd/m/yy	X%	TC 500	500	7.30	185	400	3.7	51%
Large	dd/m/yy	X%	TC 125	125	2.90	283	611	1.1	38%
Small	dd/m/yy	X%	TC 125	125	1.90	201	395	1.1	58%
Large	dd/m/yy	X%	TC 250	250	6.00	276	609	2.2	37%
Small	dd/m/yy	X%	TC 250	250	3.70	186	397	2.1	57%
Large	dd/m/yy	X%	TC 750	750	18.30	274	611	7.2	39%
Small	dd/m/yy	X%	TC 750	750	11.00	190	398	6.1	55%
Large	dd/m/yy	X%	TC 1000	1000	24.40	276	612	9.2	38%
Small	dd/m/yy	X%	TC 1000	1000	14.60	187	399	7.4	51%

Below is an example table of CDM qualification / quarterly verification waveform parameters to be recorded for the software voltage adjustment method.

Table 6. Example Waveform Parameter Recording Table for the Software Voltage Adjustment Method

Tester - System #2									
Polarity = Positive		Scope Bandwidth = 8 GHz				Factor/Offset Final Setting = 1/0			
MODULE SIZE	DATE	%RH	Test Cond	Software voltage	$I_{P\ AVG}$ (A)	$T_{R\ AVG}$ (ps)	$T_{D\ AVG}$ (ps)	$I_{P2\ AVG}$ (A)	I_{P2} (% I_{P1})
Large	dd/m/yy	X%	TC 500	410	12.1	275	610	4.3	36%
Small	dd/m/yy	X%	TC 500	410	7.30	185	400	3.7	51%
Large	dd/m/yy	X%	TC 125	105	2.90	283	611	1.1	38%
Small	dd/m/yy	X%	TC 125	105	1.90	201	395	1.1	58%
Large	dd/m/yy	X%	TC 250	205	6.00	276	609	2.2	37%
Small	dd/m/yy	X%	TC 250	205	3.70	186	397	2.1	57%
Large	dd/m/yy	X%	TC 750	620	18.30	274	611	7.2	39%
Small	dd/m/yy	X%	TC 750	620	11.00	190	398	6.1	55%
Large	dd/m/yy	X%	TC 1000	840	24.40	276	612	9.2	38%
Small	dd/m/yy	X%	TC 1000	840	14.60	187	399	7.4	51%

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ANNEX I (INFORMATIVE) – DETERMINING THE APPROPRIATE CHARGE DELAY FOR FULL CHARGING OF A LARGE MODULE OR DEVICE

This annex describes the procedure for characterizing the charge delay on the CDM tester and determining the appropriate delay (for full charging) as either the default delay for the system (if the initial large verification module checkout fails as described in Section 6.9) or the delay required for a very large package device.

I.1 Procedure for Charge Delay Determination

Follow the procedure below to determine an appropriate charge delay.

Using the large verification module or the ground pin of a very large package device:

1. Set the field plate voltage at + 250 volts (any voltage can be used as the objective is to monitor Ip).
2. With the pre/post charge delay set to 0 ms, collect 10 waveforms and record the Ip from each. Calculate the average Ip of the waveforms.
3. Increase the pre-charge delay by 50 ms, collect 10 waveforms, record the Ip from each, and calculate their average Ip.
4. Continue incrementing the delay by 50 ms (a larger or smaller step can be chosen) and record the average Ip until a minimum of 500 ms charge delay.
5. Plot the results as shown below in Figure 11.
6. The appropriate charge delay results in a “saturation point” for the Ip. As shown below in Figure 11, the Ip for this example saturates at ~300 ms. Adding some guardband to this example would ensure a pre-charge delay of 400 ms would be sufficient as either the default charge delay on the system (if the large verification module had been used) or as the required charge delay on a specific large package device if a large device had been used as the vehicle for the data collection.
7. For most large devices, it is expected that 500 ms will be sufficient to reach a saturation point. However, if after 500 ms, a saturation point has not been reached, repeat steps 4 & 5 until this occurs.
8. It is important to note that longer delay times do not “overcharge” the device but would only increase test time.

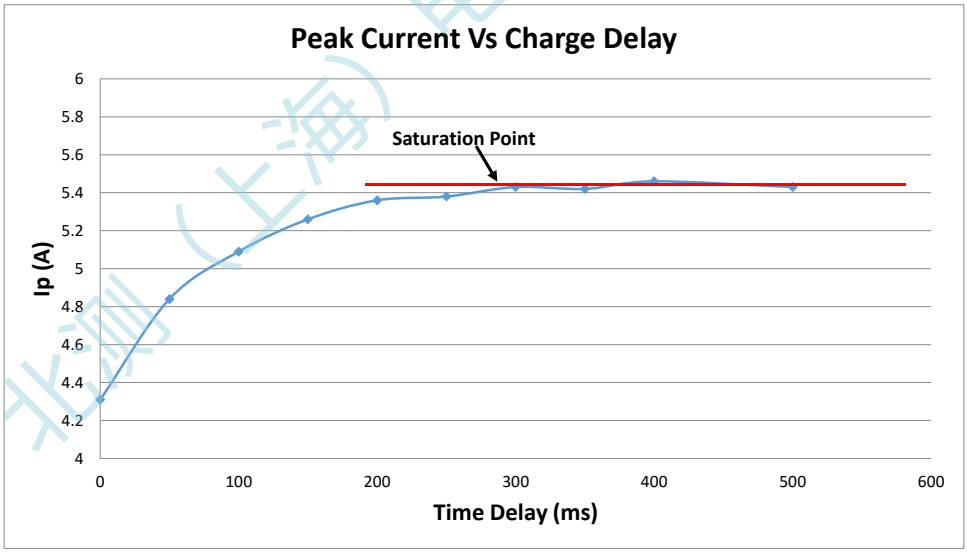

Figure 11: Example Characterization of Charge Delay vs Ip

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2018)

ANNEX J (INFORMATIVE) – ANSI/ESDA/JEDEC JS-002 REVISION HISTORY

J.1 Joint Document Summary

The initial version of this standard was a combination of ANSI/ESD S5.3.1-2009 and JESD22 – C101F. It was intended to replace these and all previous versions. The merged document contains many essential elements of both documents and hardware / measurement modifications as outlined in this section.

J.2 ANSI/ESDA/JEDEC JS-002-2014: Summary by Section

1.0 Scope and Purpose – The scope and purpose of the two documents were merged.

2.0 Referenced Documents – The previous ESDA and JEDEC methods were referenced. The ESDA and JEDEC Glossaries were referenced.

3.0 Definitions – Definitions from ESDA and JEDEC Glossary of Terms were used as appropriate.

4.0 Personnel Safety – this was made its own main section to follow the Definitions section.

5.0 Apparatus and Required Equipment – This section was re-written. Descriptions of oscilloscope and current transducers were refined. The CDM tester hardware and circuit schematic descriptions were rewritten and improved.

6.0 Stress Test Equipment Qualification and Routine Verification – This section was completely re-written. The waveform parameters Section 6.7 now contains 1 GHz and high bandwidth (>= 6 GHz) oscilloscope waveform parameters. A procedure for determining if a module or device needed a pre-charge delay setting for full module / device charging was written and references an Informative Annex H (below).

7.0 Classification Procedure – The basic procedure for sampling, pin combinations and stressing were similar in both documents. Conditions for humidity were refined. The failure criterion that was previously in its own section in both documents was moved into this section. A reporting section was also added.

8.0 Classification Criteria – This section was rewritten to restate classification levels in terms of Test Conditions. A 750-volt level was added.

Annexes

A – This Normative Annex contains verification module specifications from the JEDEC JESD22-C101F document.

B – This Normative Annex describes capacitance measurement for the small and large JEDEC style verification modules (metal discs) measurement.

C – A new Informative Annex describing the major document changes and reasoning for them was written.

D – A new Informative Annex describing the major elements of the CDM tester electrical schematic was created.

E – This is a new Informative Annex regarding the oscilloscope setup for CDM measurement.

F – This new Informative Annex describes the single and dual discharge procedures. This information was moved from the CDM Test Procedure sections of ESDA and JEDEC standards.

G – A new Informative Annex was added describing waveform verification procedures based on Test Condition voltage settings.

H – A new Informative Annex was added describing the procedure for determining any added pre-charge delay needed to fully charge a device.

I – A revision history Annex was created.

J.3 ANSI/ESDA/JEDEC JS-002-2018: Summary by Section

3.0 Definitions – Definition for C_{Small} was added.

5.2.1 Cable Assemblies – The frequency value was changed to 5 GHz.

6.5.1 CDM Test Qualification/Re-Qualification Procedure – Clarified to only use Table 2.

7.1 Tester and Device Preparations – Section title changed and sub-sections 7.1.3 and 7.1.4 were added to the document to clarify cleaning of devices and testers.

7.4 CDM Test Recording / Reporting Guidelines – This section was divided into two subsections - 7.4.1 CDM Test Recording and 7.4.2 CDM Reporting Guidelines.

7.5 Testing of Devices in Small Packages – This section was added to the document.

Annexes

Annex A – "shall" changed to "should" in a note.

Annex C – A new normative annex was created.

Subsequent annexes were re-numbered accordingly.