# JEDEC STANDARD

# Test Method for Real-Time Soft Error Rate

## JESD89-1A

Addendum No. 1 to JESD89
(Revision of JESD89-1, June 2004)

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**


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# TEST METHOD FOR REAL-TIME SOFT ERROR RATE

(From JEDEC Board Ballot JCB-07-87, formulated under the cognizance of the JC-14.1 Subcommitee on Reliability Test Metods for Packaged Devices.)

## 1 Scope

This test is used to determine the Soft Error Rate (SER) of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) for errors which require no more than re-reading or re-writing to correct and as used in terrestrial environments. It simulates the operating condition of the device and is used for qualification, characterization, or reliability monitoring. This test is intended for execution in ambient conditions without the artificial introduction of radiation sources.

JESD89-1 is offered to define concisely the requirements for executing this test in a standardized fashion. It is intended for use in conjunction with JESD89 which includes background on reasons for these requirements.

NOTE 1 Typically, soft error rate characterization by this test method will be executed by the device manufacturer. Other parties may also apply this method appropriately in conjunction with the manufacturer's product data sheet.

NOTE 2 The term real-time soft-error rate (RTSER) is preferred over the term system soft-error rate (SSER).

NOTE 3 Special considerations apply to devices that are more than memory arrays and/or bistable logic elements. These can preclude the application of this test procedure. Refer to JESD89 for further discussion on some examples.

### 1.1 Applicable documents

| | |
|---|---|
| JESD89 | Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices |
| JESD89-2 | Test Method for Alpha Source Accelerated Soft Error Rate |
| JESD89-3 | Test Method for Beam Accelerated Soft Error Rate |
| JESD22-A108 | Temperature, Bias, and Operating Life |

## 2 Apparatus

The performance of this test requires equipment that is capable of providing the particular test conditions to which the test samples will be subjected. (As a practical matter, this equipment will typically provide the means to collect data on many samples under evaluation over the same time period.)

The integrity of the test apparatus shall be verified prior to data collection. The particulars of the verification process are left to the individual investigator for their specific equipment.

### 2.1 Vehicle design and operation

The circuitry through which the samples shall be biased shall be designed with the following considerations:

The biasing and operating schemes shall consider the limitations of the device and shall not overstress the devices or contribute to thermal runaway.

The test circuit shall be designed to limit power dissipation such that if a device failure occurs, excessive power cannot be applied to other devices in the sample.

### 2.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under test, (e.g., improper heat dissipation).

### 2.3 Power supplies and signal sources

Instruments (e.g., oscilloscopes) used to set up and monitor power supplies and signal sources shall be calibrated and have long-term stability. Electrical noise shielding shall be in place to allow for accurate test results.

## 3 Terms and definitions

**absolute maximum rated temperature:** The maximum junction or ambient temperature of an operating device as listed in its data sheet and beyond which damage (latent or otherwise) may occur. It is frequently specified by device manufacturers for a specific device and/or technology.

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

**absolute maximum rated voltage**: The maximum voltage that may be applied to a device and beyond which damage (latent or otherwise) may occur. It is frequently specified by device manufacturers for a specific device and/or technology.

**critical charge (Qcrit):** The minimum amount of collected charge that will cause the node to change state..

**hard error:** An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit (e.g., gate oxide rupture, destructive latch-up events).

NOTE The error is called “hard” because the data is lost and the circuit or device no longer functions properly, even after power reset and re-initialization.

**minimum operating voltage:** The minimum power supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

## 3 Terms and definitions (cont'd)

**multiple-bit upset (MBU):** A multiple-cell upset (MCU) in which two or more error bits occur in the same word.

NOTE An MBU cannot be corrected by a simple (single-bit) ECC.

**multiple-cell upset (MCU):** A single event that induces several bits in an IC array to fail at the same time.

NOTE The error bits are usually, but not always, physically adjacent.

**real-time soft error rate (RTSER); system soft error rate (SSER):** The soft error rate in a naturally occurring alpha particle and neutron environment.

NOTE 1 The RTSER is measured using a large number of devices to obtain a statistically significant error count, in contrast to an accelerated SER test where an intense radiation source is used on a single device or small number of devices.

NOTE 2 The RTSER error counts can be increased by using a higher neutron flux at higher altitudes, but for the purposes of this specification, the term "accelerated" is reserved for intense radiation sources that do not occur in natural terrestrial environments.

**single-event burnout (SEB):** An event in which a single energetic-particle strike induces a localized high-current state in a device that results in catastrophic failure.

**single-event effect (SEE):** Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic-particle strike.

NOTE Single-event effects include single-event upset (SEU), multiple-bit SEU (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE), single-event transient (SET), single-event burnout (SEB), and single-event gate rupture (SEGR).

**single-event functional interrupt (SEFI):** A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).

NOTE An SEFI is often associated with an upset in a control bit or register.

**single-event gate rupture (SEGR):** An event in which a single energetic-particle strike results in a breakdown and subsequent conducting path through the gate oxide of a MOSFET.

NOTE An SEGR is manifested by an increase in gate leakage current and can result in either the degradation or the complete failure of the device.

**single-event hard error (SHE):** An irreversible change in operation resulting from a single radiation event and typically associated with permanent damage to one or more elements of a device (e.g., gate oxide rupture).

## 3 Terms and definitions (cont'd)

**single-event latch-up (SEL):** An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.

NOTE 1 SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.

NOTE 2 An example of SEL in a CMOS device occurs when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

**single-event transient (SET):** A momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by the passage of a single energetic particle.

**single-event upset (SEU):** A soft error caused by the signal induced by the passage of a single energetic particle.

**soft error, device:** An erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell.

NOTE 1 As commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process.

NOTE 2 Soft errors can be generated from SEU, SEFI, MBU, MCU, and/or SET. The term SER, which includes a variety of soft error mechanisms, has been adopted by the commercial industry while the more specific terms SEU, SEFI, etc. are typically used by the avionics, space, and military electronics communities.

**soft error, power-cycle (PCSE):** A soft error that is not corrected by repeated reading or writing but can be corrected by the removal of power (e.g., nondestructive latch-up).

**soft error, static:** A soft error that is not corrected by repeated reading but can be corrected by rewriting without the removal of power

**soft error, transient:** A soft error that can be corrected by repeated reading without rewriting and without the removal of power.

# 4 Procedure

## 4.1 Test duration

The test duration shall be specified by internal qualification requirements or the applicable procurement document.

The test duration is defined as the time from the first data write at test conditions to the last read at test conditions. The time spent performing any chamber setup and power down shall not be considered a portion of the total specified test duration.

## 4.2 Test conditions

### 4.2.1 Temperature

Unless otherwise specified, the junction temperature for the devices under evaluation shall be controlled to within a tolerance of +/-10°C of each other. (A junction temperature of 40°C is recommended where guidance is needed; other junction temperature conditions may be dictated by customer specification or technical constraints.)

### 4.2.2 Operating voltage

Unless otherwise specified, the operating voltage shall be the nominal operating voltage specified for the device. In order to characterize SER as a function of Qcrit, a lower/higher voltage is permitted. This voltage shall not exceed the absolute maximum rated voltage for the device and shall be agreed upon by the device manufacturer.

Care shall be taken in all cases to understand what the device operating voltages are in either bypass mode or regulated mode.

### 4.2.3 Biasing configurations

The parts shall be operated in a dynamic mode during the life test consistent with those described for High Temperature Operating Life (HTOL) in JESD22-A108. Device outputs may be unloaded or loaded to achieve the specified output voltage level. If a device has a thermal shutdown feature, it shall not be biased in a manner that could cause the device to go into thermal shutdown.

#### 4.2.3.1 Real-Time SER test

Unless otherwise stated, the RTSER test shall be configured to provide write/read function to the entire available array of the device samples with insitu pass/fail recording. The cumulative time in each valid data state for each memory array element shall be approximately equal, i.e., a two-state memory element shall see equal cumulative time over the RTSER test in the high state and the low state. It is recommended that the patterns or pattern suite otherwise approximate typical use.

For characterization purposes test conditions can be modified. These include supply voltages, clock frequencies, input signals, etc., which may be operated outside their specified values. When operating outside the application range of the part, predictable and nondestructive behavior of the devices under test shall be assured.

### 4.3 Test readiness

Prior to running the SER test, a tester readiness check shall be performed. This check shall be performed with the hardware in the manner it will be used for the test. The parts shall be operated to the basic write/read pattern that will be used for the test. The check is completed successfully when no parts fail the basic write/read pattern.

This check shall be performed before any test in which the test setup was changed.

### 4.4 Handling

All testing shall follow appropriate procedures for safe handling and ESD control.

## 5 Measurements

The RTSER test requires that the output of each device be monitored and checked against the expected result in a manner such that the time between reads is less than 0.10 of the mean time between errors. This frequency is intended to help distinguish between multiple errors caused by a single event and multiple errors caused by multiple events.

## 6 Failure criteria

Any result that does not match expectation is a possible soft error and shall be recorded. If a possible error is identified, action should be taken to verify that it is a soft error.

Care shall be taken to minimize electrically noisy test environments and, thereby, errors related to the equipment and not the device.

Consideration shall be given to discriminating among the error types which can be encountered.

To distinguish a soft error in the device from a soft error during the system read, the data shall be read more than once at each readout. An error which is not consistently observable through repeated reading shall be considered a “transient” soft error. A soft error which remains uncorrected by additional reading without re-writing shall be considered a potential “static” soft error.

To differentiate among static soft errors, power-cycle soft errors (PCSE), and single-event hard errors (SHE), data shall be rewritten into the device and re-read. If the error is corrected by re-writing, it shall be recorded as a static soft error. If the error repeats after re-writing, it is not a static soft error. When an error persists after re-writing, the chip shall undergo a power cycle where the power is removed then restored. After the power-cycle, both data states shall be written into and re-read from the faulting bits. Any faulting bits that can be written into both states and re-read from both data states without error after power-cycle shall be recorded as power-cycle soft errors. Faults which persist after writing into or re-reading either data state after power-cycle shall be recorded as hard errors. PCSE and SHE shall not be counted as static or transient soft errors

## 6 Failure criteria (cont'd)

Any soft error that affects multiple cells in a single read period through the memory array --and that cannot be otherwise demonstrated to be a set of independent cell errors -- shall be reported as a multiple-cell error and classified and counted according to its failure signature. The independence of cell errors can be demonstrated by distinct separation in the time of occurrence, established separation of failing physical addresses, and/or independence of the local array controls and supports for the affected cells.

NOTE An assessment of fault independence based on a distinction of tester timestamps shall consider the delay time between the event and read record. (For example, two errors caused by the same event can have different tester timestamps depending on when they are read within the read cycle of the entire chip and when the event happens within that read cycle.)

Where possible, it is desirable to identify the subset of PCSE that are SEL (as by measurement of anomalous current). Likewise where possible, it is desirable to identify the subset of static or transient soft errors that are SEFI. For memory arrays, SEFI may be distinguishable by the extent of related array addresses that are affected (as in an entire array or array subset dependent on operation of a common latch).

## 7 Report

The following items shall be contained in the final report for any RTSER test:

1. Sample size (number of devices tested)
2. Amount of array or bistable logic elements tested per device
3. Supplier, supplier part number, and die revision (if applicable)
4. Circuit type (e.g., SRAM, DRAM, etc.)
5. ECC description (type and coverage) or "tested per data sheet, ECC unknown"
6. Package description (e.g., connection to chip, materials, geometries) with description of any modifications made for SER testing
7. Test duration
8. Portion of test duration that is cumulative 'dead' (untested) time (Time that is untested between a read followed by a write)
9. Calendar dates and times for data collection
10. Voltage (external supply, use of internal regulated, back bias if applicable)
    NOTE Reporting an internal regulate voltage level is optional, but encouraged where the portability of the date to other devices is of interest.
11. Temperature during test (at minimum, ambient temperature; if available, junction temperature as well)
12. Core cycle time or frequency or designation as "static" test with special notation of cycle times different than product data sheet
13. Refresh rate, where applicable
14. Test pattern(s), including the logical data pattern and, if known, the physical data pattern
15. Tester (commercial model and/or physical description)

## 7 Report (cont'd)

16. Test board description
17. Special shielding from radiation sources, if any
18. Stacking or other multi-device configurations used during testing
19. Problems or unusual behavior of the devices during test
20. Fail information:
    a. Count of each soft error type (transient soft errors, static soft errors)
    b. Calendar date and time of each error
    c. Identification of those soft errors that are multiple-cell errors
    d. Failing logical address or addresses
       NOTE Interpretation of multi-cell errors is enhanced by an understanding of the physical relationship of failing addresses
    e. Test conditions (voltage, ECC usage, data pattern, etc.) where multiple conditions are applied within the same RTSER
    f. Failure rate in test condition. Ideally, the failure rate should should be identified on both a per-bit (or other circuit element) basis as well as a per-event basis. At minimum, the basis for any given failure rate shall be clearly identified.
21. Location of devices under test, including
    a. Latitude and longitude
    b. Altitude
    c. General building description and location within building (e.g., 1 floor below ground level in a 2-story industrial/commercial building of brick construction)
22. Average atmospheric conditions for test period
23. Periodicity of test readouts
24. Angular orientation with respect to ground level during test of the chip active surface (if known) or the packaged device (if the chip active surface orientation is unknown)

If available, it is recommended to document the following information:

A. Dimensions of active area tested
B. Process technology features (e.g., lithographic node, number and type of metal levels, post-metal insulators like polyimide)

## Annex A (informative) Differences between JESD89-1A and JESD89-1

This table briefly describes most of the changes made to entries that appear in this standard, JESD89-1A, compared to its predecessor, JESD89-1 (June 2004). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

**Page** **Description of change**

At time of publication a change page was not provided.

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